Compal LA-G741P

KBL-U/R MB Schematic Document

Pantheon

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Security Classification	Compal Secret Data		
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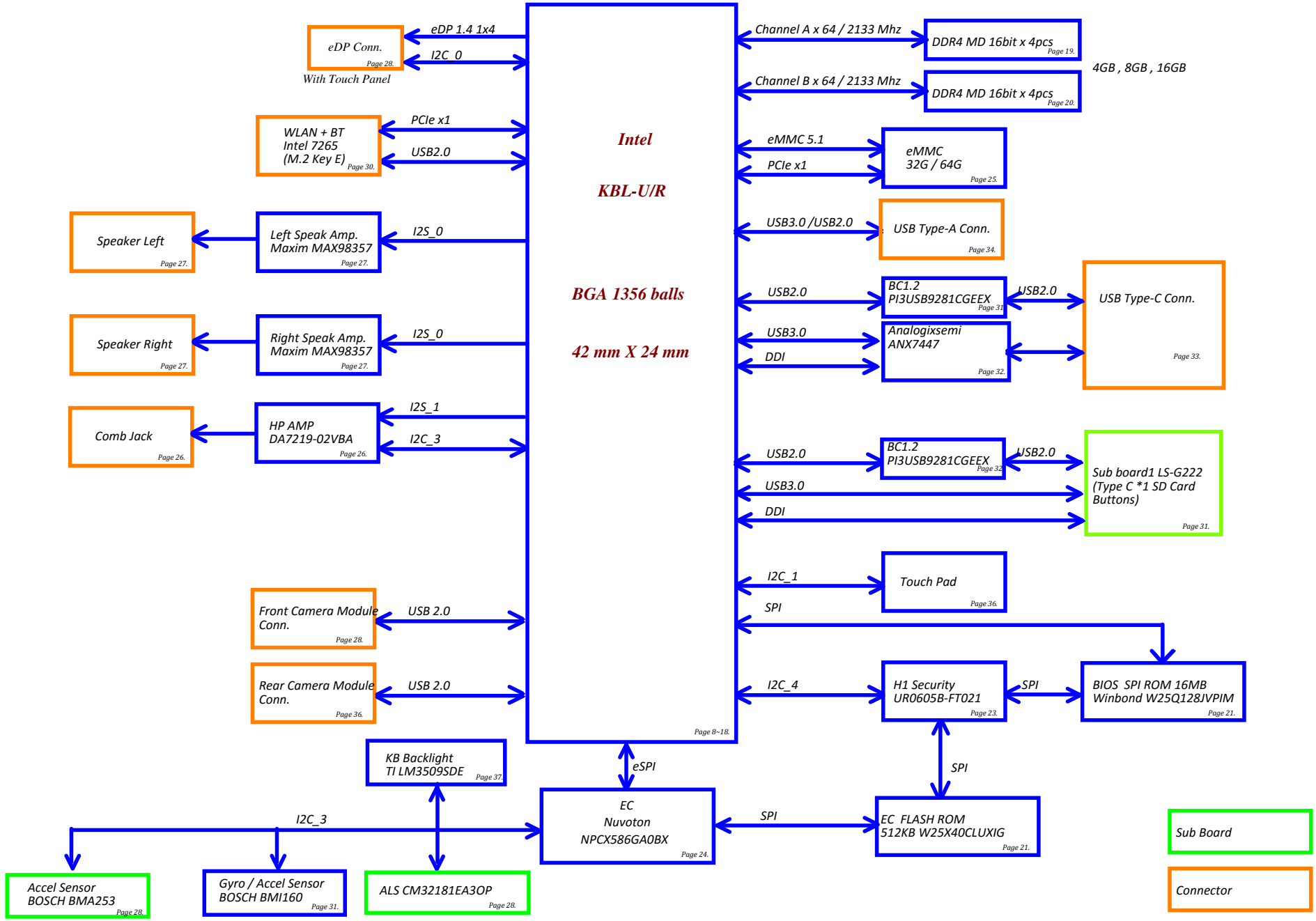

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Title	Block Diagram		
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Intel KBL-U Platform		KBL-U Chromebook (EQA04)		
HSIO Port	Capable	Port Allocation	PCIE CLK & CLKREQ	Note
1	USB3 #1 / OTG	USB3 Type-C port 0		
2	USB3 #2 / SSIC	USB3 Type-C port 1		
3	USB3 #3	USB3 Type-A port 0		
4	USB3 #4	USB3 to SD card reader		
5	PCIE #1 / USB3 #5			
6	PCIE #2 / USB3 #6			
7	PCIE #3 / LAN	NA		
8	PCIE #4 / LAN	WLAN + BT Intel 7265	PCIE CLK 1	M.2 key-E
9	PCIE #5 / LAN	SSD (PCIe x4/SATA)	PCIE CLK 3	M.2 key-E
10	PCIE #6			
11	SATA #0 / PCIE #7			
12	SATA #1 / PCIE #8			
13	PCIE #9 / LAN	On board NVMe	PCIE CLK 2	
14	PCIE #10 / LAN	On board NVMe	PCIE CLK 2	
15	PCIE #11			
16	PCIE #12			

Intel KBL-U Platform		KBL-U Chromebook (EQA04)	
USB Port	Capable	Port Allocation	Note
1	USB2 #1	USB3 Type-C port 0	
2	USB2 #2	USB3 Type-C port 1	
3	USB2 #3	USB3 Type-A port 0	
4	USB2 #4	USB3 to SD card	
5	USB2 #5	BLUETOOTH ON M.2	
6	USB2 #6	CAMERA 1	Rear
7	USB2 #7	CAMERA 2	Front
8	USB2 #8		
9	USB2 #9	M.2 key-E	
10	USB2 #10	NA	

Intel KBL-U Platform		KBL-U Chromebook (EQA04)	
DDI Port	Capable	Port Allocation	Note
1	DDI #1	Type-C port 1	
2	DDI #2	Type-C port 0	

SOC			
I2C Port	Voltage level	Device	Address(7 bit)
I2C_0	3.3V	Touch Screen	
I2C_1	3.3V	Trackpad	0011001
I2C_2	3.3V	Active pen	
I2C_3	1.8V	Headphone codec	0011010
I2C_4	3.3V	H1(Reserve)	

SOC	
GPIO group	Votagle level
A	1.8V
B	3.3V
C	3.3V
D	1.8V
E	3.3V
F	1.8V
G	3.3V

EC			
I2C Port	Power Rail	Device	Address(7 bit)
I2C_0	3.3V	BC1.2 Detecter (USB-C Port 0)	0100101
	3.3V	TCPC & Redrive-MUX (USB-C Port 0)	0001011
I2C0_1	3.3V	BC1.2 Detecter (USB-C Port 1)	0100101
		TCPC & Redrive-MUX (USB-C Port 1)	0101011
I2C_1	3.3V	Battery	0010110
I2C_2	3.3V	KB Back Light (LM3509)	0110110
	3.3V	PMIC	0110000
	3.3V	Battery Charger	0001001
I2C_3	3.3V	6-axis Accel & Gyro	1101000
		ALS	1000100
		G-sensor	0011000
		Thermal Sensor(F75303M_MSOP10)	1001100

	Location	Address	Channel	Test_Power_Net_Name	Test_Point		Remark
INA3221AIRGVR	U35	1000000	CH1	PPVAR_SYS_PMIC_V1	PR127	0.01_0603_1%	PP1000_A Source
			CH2	PPVAR_BL_PWR	F1	0.005_2010_1%	Panel backlight
			CH3	PPVAR_VCC	PR87	0.01_1206_1%	PPVAR_VCC Source
	U36	1000001	CH1	PP5000_A	PR160	0.005_1206_1%	
			CH2	PPVAR_SYS_PMIC_V5	PR159	0.01_0805_1%	PP5000_A Source
			CH3	PP1800_A	PR137	0_0603_5%	
	U37	1000010	CH1	PP1200_VDDQ	PR152	0.005_1206_1%	
			CH2	PP0600_DDRVTT	PR929	0.01_0603_1%	
			CH3	SYS_PPVAR_SYS_PMIC_V4	PR151	0_0603_5%	PP1200_VDDQ Source
	U38	1000011	CH1	VINVR2_650830	PR1236	0_0402_5%	PP1800_A Source
			CH2	PP1200_VDDQ_DDRVTTIN	PR931	0_0402_5%	PP0600_DDRVTT Source
			CH3	PPVAR_SYS_PMIC_V3	PR140	0.01_0805_1%	PP3300_DSW Source
INA219AIDCNRG4	U39	1000100	CH1	+8.4VB_VCC2_VIN	PR92	0.01_1206_1%	PPVAR_VCC Source
	U40	1000110	CH1	PP3300_DSW	PR138	0.005_1206_1%	
	U41	1001000	CH1	PPVAR_GT_VIN	PR97	0.01_1206_1%	PPVAR_GT Source
	U42	1000111	CH1	PPVAR_PWR_IN_BB	PR1	0.02_1206_1%	Charger
	U44	1000101	CH1	PPVAR_SA_VIN	PR99	0.01_1206_1%	PPVAR_SA Source
	U97	1001001	CH1	PP3300_S	R4920	0.01_0603_1%	
	U98	1001010	CH1	PP3300_DX_WLAN	R381	0.01_0805_1%	
	U99	1001011	CH1	PP1000_A	PR128	0.005_1206_1%	
	U100	1001100	CH1	PP3300_DX_EDP	R378	0.01_0603_1%	
	U101	1001101	CH1	PP3300_DSW_EC	R271	0.01_0402_1%	

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EQA04/Nami

Schematic:
LA-G222PR02

PVAR_SYS

VR / Load SW	Power Rail Name	VR / Load SW	Power Rail Name	VR / Load SW	Power Rail Name	VR / Load SW	Power Rail Name
= PMIC = Load switch		= Resistor		= Power rail for SoC = Power rail for device			

PU2
ISL95857 (IMVP8 VR)
EN: ALL_SYS_PWRGD
→ PPVAR_VCC
→ PPVAR_GT
→ PPVAR_SA

PU901
G922T11U
EN:PPVAR_SYS
→ PP3300_H1

PU7
TPS65983ZCGR [VR1]
EN: PP3300_A_PCH_PG
@EC_ROP_SLP_SUS#
PP1000_A →
UC5
APE8939GN3
EN: EN_VCCSTG_VCCPLL_OC
@EN_PP1000_VCCSTG
→ PP1000_VCCSTG

UC4 (CH1)
EM5209VF
EN:PM_SLP_S4#
→ PP1000_VCCSTU
RC24 0 ohm → PP1000_VCCST
RC28 0 ohm → PP1000_VCCSFR

PU7B
TPS65083ZCGR [VR3]
EN:ROP_PMIC_ENVR3
PP3300_DSW →
UC7(CH1)
JW7110DFNC
EN:EN_PP3300_A
@EC_ROP_SLP_SUS#
→ PP3300_A
RC51 0 ohm → PP3300_SOC_A
RC45 0 ohm → PP1800_3300_PGPPD
RC50 0 ohm → PP3300_PGPPG
R4919 0 ohm → PP3300_S_TRACKPAD

U50
TPS22913CYZVR
EN:EN_PP3300_DX_EDP
→ PP3300_DX_EDP
U46
TPS22913CYZVR
EN: EN_PP3300_DX_CAM
→ PP3300_DX_CAM1

U52
TPS22914CYFPR
EN:EN_PP3300_DX_WLAN
→ PP3300_DX_WLAN
U63
TPS22913CYZVR
EN: EN_PP3300_DX_CAM
→ PP3300_DX_CAM2

U53
TPS22913CYZVR
EN: EN_PP3300_USB_PD
→ PP3300_USB_PD
U93
SLG5NT1477VTR
EN:PM_SLP_S3#
→ PP3300_S
R405 0 ohm → PP3300_S_SSD
R955 0 ohm → PP3300_S_EMMC
R395 0 ohm → PP3300_S_PEN

R271
0.01 ohm
→ PP3300_DSW_EC
R953 0 ohm → PP3300_DSW_SENSOR

R4943
0 ohm
→ PP3300_S_TOUCHSCREEN

U43
G9090-180T11U
EN:PP3300_DSW
→ PP1800_DSW
R914 0 ohm → PP3300_DSW_SENSOR

PU8
G9661MF11U
EN:PM_SLP_S4#
→ PP2500_DRAM

PU7B
TPS65083ZCGR (VR2)
EN:EC_ROP_SLP_SUS#
→ PP1800_A
RC33 0 ohm → PP1800_HDA_A
UC4 (Ch2)
JW7110DFNC
EN: PM_SLP_S3#
→ PP1800_S
R913 0 ohm → PP1800_S_EMMC
R394 0 ohm → PP1800_S_PEN
RC46 0 ohm → PP1800_3300_PGPPD

PU7C
TPS65083ZCGR (VR4)
EN: PM_SLP_S4#
PP1200_VDDQ →
RC20/RC223
0.01 ohm
→ PP1200_VDDQ_SOC
RC31 0.01 ohm → PP1200_VDDQC
UC7(CH2)
JW7110DFNC
EN:EN_VCCSTG_VCCPLL_OC
@PM_SLP_S3#
→ PP1200_VCCSFR_OC

PU7C
TPS65083ZCGR (LDO1)
→ PP0600_DDRVTT

PU7C
TPS65083ZCGR (VR5)
EN:EC_ROP_SLP_SUS#
→ PP5000_A

PU902
TPS65261RHBR
EN:PM_SLP_S3#
→ PP3300_S_NVME

PU902
TPS65261RHBR
EN:PM_SLP_S3#
→ PP1800_S_NVME

PU902
TPS65261RHBR
EN:PM_SLP_S3#
→ PP1100_S_NVME

PU7A
TPS65083ZCGR
→ PP3300_RTC

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Title: Power Map

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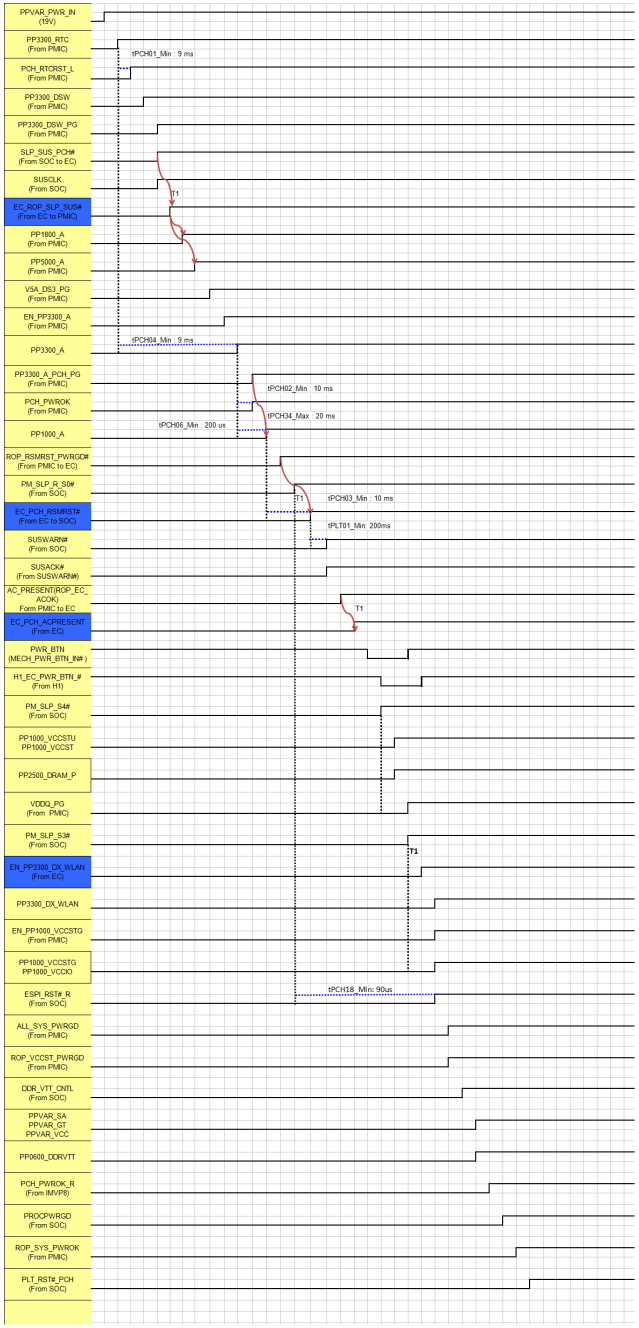

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M/B Sku #	RAM/SoC	Load BOM option (Stuff)	Load BOM option (DNS)
1	SAMSUNG_4G/Celeron	Celeron@/SAMSUNG_4G@/SANDISK_32G@/XDP@/EMI@/U22@/RF@/MP@/INA@/ESPI@/ESD@/EMMC@/DSX_S0IX@/DSX@/SDP@	@/@RF@/@EMI@
2	SAMSUNG_4G/Pentium	Pentium@/SAMSUNG_4G@/SANDISK_32G@/XDP@/EMI@/U22@/RF@/MP@/INA@/ESPI@/ESD@/EMMC@/DSX_S0IX@/DSX@/SDP@	@/@RF@/@EMI@
3	SAMSUNG_8G/U-i3	U_i3@/SAMSUNG_8G@/SAMSUNG_32G@/XDP@/EMI@/U22@/RF@/MP@/INA@/ESPI@/ESD@/EMMC@/DSX_S0IX@/DSX@/SDP@	@/@RF@/@EMI@
4	SAMSUNG_8G/R-i5	R_i5@/SAMSUNG_8G@/SAMSUNG_32G@/XDP@/EMI@/U42@/RF@/MP@/INA@/ESPI@/ESD@/EMMC@/DSX_S0IX@/DSX@/SDP@	@/@RF@/@EMI@
5	HYNIX_16G/R-i7	R_i7@/HYNIX_16G@/SANDISK_64G@/XDP@/EMI@/U42@/RF@/MP@/INA@/ESPI@/ESD@/EMMC@/DSX_S0IX@/DSX@/DDP@	@/@RF@/@EMI@
6	SAMSUNG_8G/R-i3	R_i3@/SAMSUNG_8G@/SAMSUNG_32G@/XDP@/EMI@/U42@/RF@/MP@/INA@/ESPI@/ESD@/EMMC@/DSX_S0IX@/DSX@/SDP@	@/@RF@/@EMI@
7	SAMSUNG_8G/U-i5	U_i5@/SAMSUNG_8G@/LONGSYS_128G@/XDP@/EMI@/U22@/RF@/MP@/INA@/ESPI@/ESD@/DSX_S0IX@/DSX@/SDP@/NVME@	@/@RF@/@EMI@

[PCB]

ZZZ

PCB 2DB LA-G741P REV0 M/B 2

DAA000HF010

SOC

UC1 — KBL-R I3-8130U
S IC FJ8067703282227 SR3W0 Y0 2.2G FCBGA
KBLR_I3@
SA0000BWN30

UC1 — KBL-R I5-8250U
S IC FJ8067703282221 SR3LA Y0 1.6G FCBGA
KBLR_I5@
SA0000AWB50

RAM ID

Vendor	Vendor P/N	Memory	Channel	[3]	[2]	[1]	[0]	BOM structure	Die Package	Stuff component
MICRON	MT40A256M16GE-083E:B	4G	2	0	0	0	1	MICORN_4G@	SDP	R89,R90,R91,R92
SAMSUNG	K4A8G165WB-BCRC	8G	2	0	0	1	0		SDP	R88,R90,R91,R93
				0	0	1	1			R88,R89,R90,R91
HYNIX	H5ANAG6NAMR-UHC	16G	2	0	1	0	0		DDP	R87,R90,R92,R93
				0	1	0	1			R90,R87,R92,R89
				0	1	1	0			R87,R88,R90,R93
SAMSUNG	K4A4G165WE-BCRC	4G	2	0	1	1	1		SDP	R87,R88,R89,R90
SAMSUNG	K4A8G165WC-BCTD	8G	2	1	0	0	0	SAMSUNG_8G@	SDP	R86,R91,R92,R93
HYNIX	H5AN4G6NAFR-UHC	4G	2	1	0	0	1	HYNIX_4G_1@	SDP	R86,R91,R92,R89
				1	0	1	0			
				1	0	1	1			
SAMSUNG	K4AAG165WB-MCRC	16G	2	1	1	0	0		DDP	R86,R87,R92,R93
				1	1	0	1			
MICORN	MT40A512M16LY-075:E	8G	2	1	1	1	0	MICORN_8G@	SDP	R86,R87,R88,R93
HYNIX	H5AN8G6NCJR-VKC	8G	2	1	1	1	1	HYNIX_8G@	SDP	R86,R87,R88,R89

eMMC

SDINADF4-32G-1001K SANDISK_32G@ SA00009W370	H26M62002JPR HYNIX_32G@ SA0000ADH10	KLMBG2JETD-B041 SAMSUNG_32G@ SA0000A7X00	SDINADF4-32G-1001 SANDISK_32G_J@ SA00009W350	SDINBDA4-32-1001V SANDISK_32G_J@ SA0000C0B00	SDINBDA4-32-1001V (R3) SANDISK_32G_A@ SA0000C0R10
KLMCG2KCTA-B041 SAMSUNG_64G@ SA0000BR900	SDINADF4-64G-1001K SANDISK_64G@ SA00009L170	H26M74002HMR HYNIX_64G@ SA0000A7100	SDINBDA4-64-1001V SANDISK_64G_1@ SA0000B4R00	SDINADF4-64G-1001K (R3) SANDISK_64G_A@ SA00009L180	SDINBDA4-64-1001V (R3) SANDISK_64G_B@ SA0000B4R10
KLMDG4UCTA-B041 SAMSUNG_128G@ SA0000BR800	DINADF4-128-1001K SANDISK_128G@ SA00009ML60	H26TB7001CMR HYNIX_128G@ SA0000BPX00	SDINBDA4-128-1001V SANDISK_128G_1@ SA0000BPN00	DINADF4-128-1001K (R3) SANDISK_128G_A@ SA00009ML70	H26TB7001CMR (R3) HYNIX_128G_B@ SA0000BPX10
SDINBDA4-128-1001V (R3) SANDISK_128G_C@ SA0000BPN10					

DDR

SAMSUNG_8G@	R86 10K_0201_1% SAMSUNG_8G@	R91 10K_0201_1% SAMSUNG_8G@	R92 10K_0201_1% SAMSUNG_8G@	R93 10K_0201_1% SAMSUNG_8G@
HYNIX_8G@	R86 10K_0201_1% HYNIX_8G@	R87 10K_0201_1% HYNIX_8G@	R88 10K_0201_1% HYNIX_8G@	R89 10K_0201_1% HYNIX_8G@
MICRON_8G@	R86 10K_0201_1% MICRON_8G@	R87 10K_0201_1% MICRON_8G@	R88 10K_0201_1% MICRON_8G@	R93 10K_0201_1% MICRON_8G@
MICRON_4G@	R89 10K_0201_1% MICRON_4G@	R90 10K_0201_1% MICRON_4G@	R91 10K_0201_1% MICRON_4G@	R92 10K_0201_1% MICRON_4G@
HYNIX_4G_1@	R86 10K_0201_1% HYNIX_4G_1@	R91 10K_0201_1% HYNIX_4G_1@	R92 10K_0201_1% HYNIX_4G_1@	R89 10K_0201_1% HYNIX_4G_1@

DDR

SDP	K4A8G165WC-BCTD SAMSUNG_8G@ SA0000B6F10	K4A8G165WC-BCTD SAMSUNG_8G@ SA0000B6F10	K4A8G165WC-BCTD SAMSUNG_8G@ SA0000B6F10	K4A8G165WC-BCTD SAMSUNG_8G@ SA0000B6F10
	K4A8G165WC-BCTD SAMSUNG_8G@ SA0000B6F10	K4A8G165WC-BCTD SAMSUNG_8G@ SA0000B6F10	K4A8G165WC-BCTD SAMSUNG_8G@ SA0000B6F10	K4A8G165WC-BCTD SAMSUNG_8G@ SA0000B6F10
SDP	H5AN8G6NCJR-VKC HYNIX_8G@ SA00000BMN10	H5AN8G6NCJR-VKC HYNIX_8G@ SA00000BMN10	H5AN8G6NCJR-VKC HYNIX_8G@ SA00000BMN10	H5AN8G6NCJR-VKC HYNIX_8G@ SA00000BMN10
	H5AN8G6NCJR-VKC HYNIX_8G@ SA00000BMN10	H5AN8G6NCJR-VKC HYNIX_8G@ SA00000BMN10	H5AN8G6NCJR-VKC HYNIX_8G@ SA00000BMN10	H5AN8G6NCJR-VKC HYNIX_8G@ SA00000BMN10
SDP	MT40A512M16LY-075:E MICRON_8G@ SA00000ARD30	MT40A512M16LY-075:E MICRON_8G@ SA00000ARD30	MT40A512M16LY-075:E MICRON_8G@ SA00000ARD30	MT40A512M16LY-075:E MICRON_8G@ SA00000ARD30
	MT40A512M16LY-075:E MICRON_8G@ SA00000ARD30	MT40A512M16LY-075:E MICRON_8G@ SA00000ARD30	MT40A512M16LY-075:E MICRON_8G@ SA00000ARD30	MT40A512M16LY-075:E MICRON_8G@ SA00000ARD30
SDP	H5AN4G6NAFR-UHC HYNIX_4G_1@ SA00009U300	H5AN4G6NAFR-UHC HYNIX_4G_1@ SA00009U300	H5AN4G6NAFR-UHC HYNIX_4G_1@ SA00009U300	H5AN4G6NAFR-UHC HYNIX_4G_1@ SA00009U300
	H5AN4G6NAFR-UHC HYNIX_4G_1@ SA00009U300	H5AN4G6NAFR-UHC HYNIX_4G_1@ SA00009U300	H5AN4G6NAFR-UHC HYNIX_4G_1@ SA00009U300	H5AN4G6NAFR-UHC HYNIX_4G_1@ SA00009U300
SDP	MT40A256M16GE-083E:B MICORN_4G@ SA00009NS00	MT40A256M16GE-083E:B MICORN_4G@ SA00009NS00	MT40A256M16GE-083E:B MICORN_4G@ SA00009NS00	MT40A256M16GE-083E:B MICORN_4G@ SA00009NS00
	MT40A256M16GE-083E:B MICORN_4G@ SA00009NS00	MT40A256M16GE-083E:B MICORN_4G@ SA00009NS00	MT40A256M16GE-083E:B MICORN_4G@ SA00009NS00	MT40A256M16GE-083E:B MICORN_4G@ SA00009NS00

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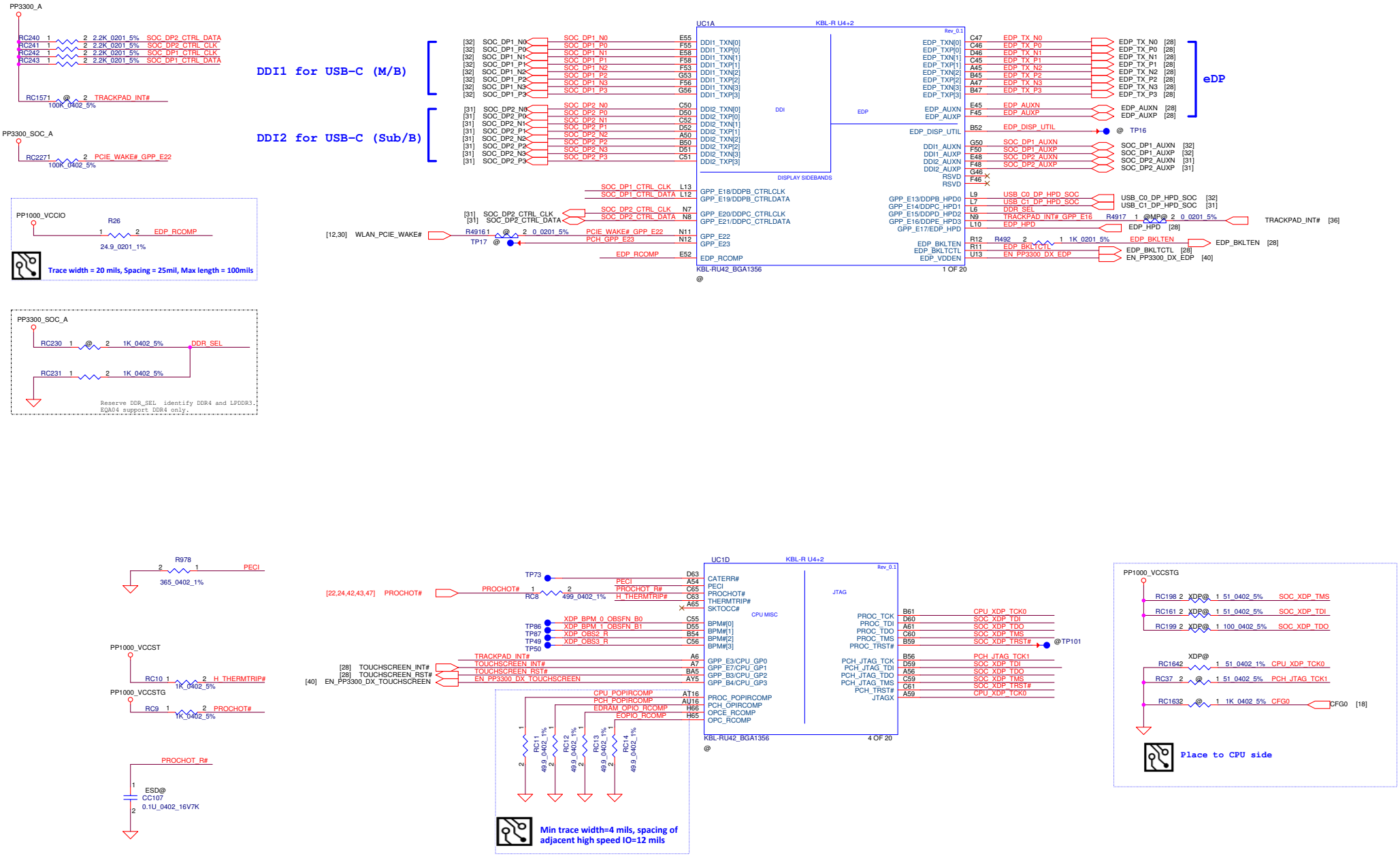

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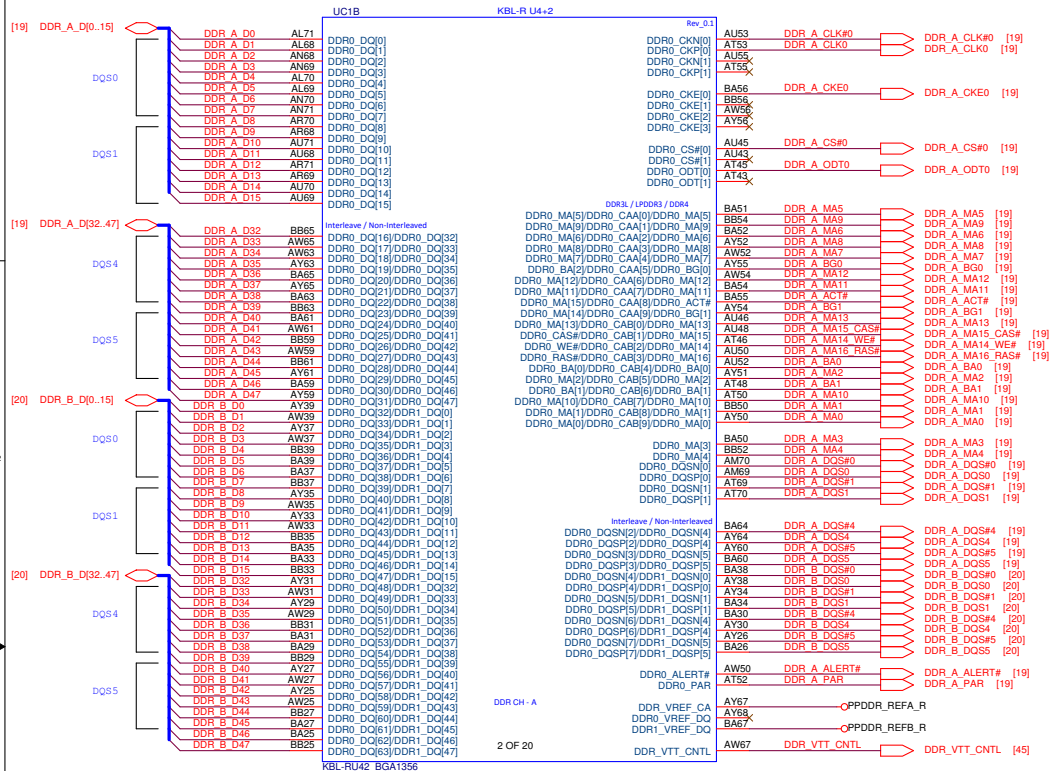
Date:	Thursday, July 19, 2018	Sheet	8 of 54



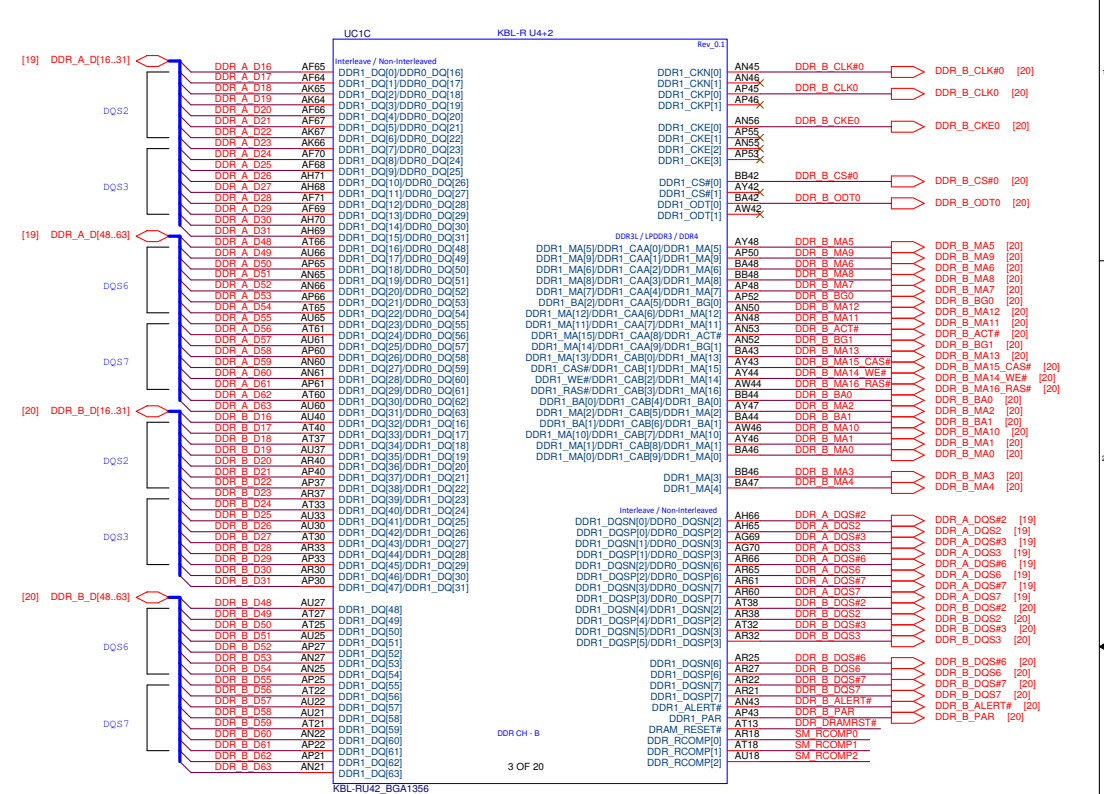
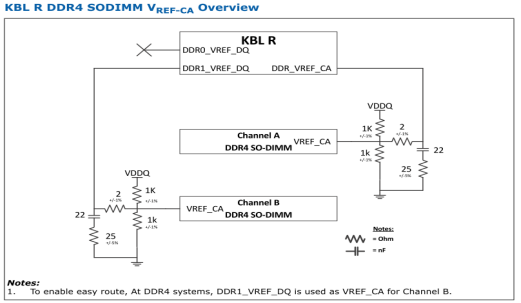
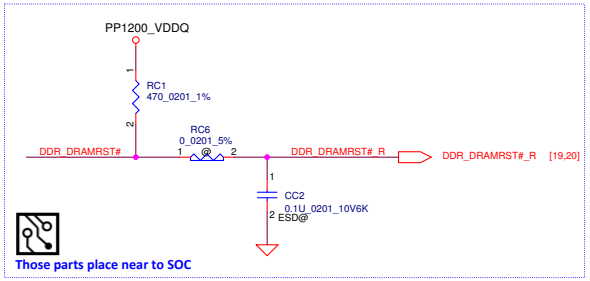
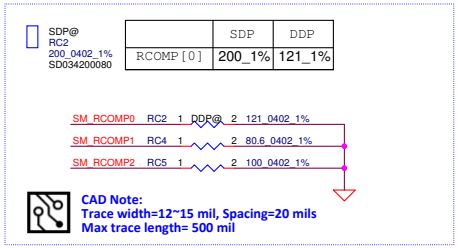


Figure 4-16. KBL R DDR4 SODIMM V_{REF-CA} Overview







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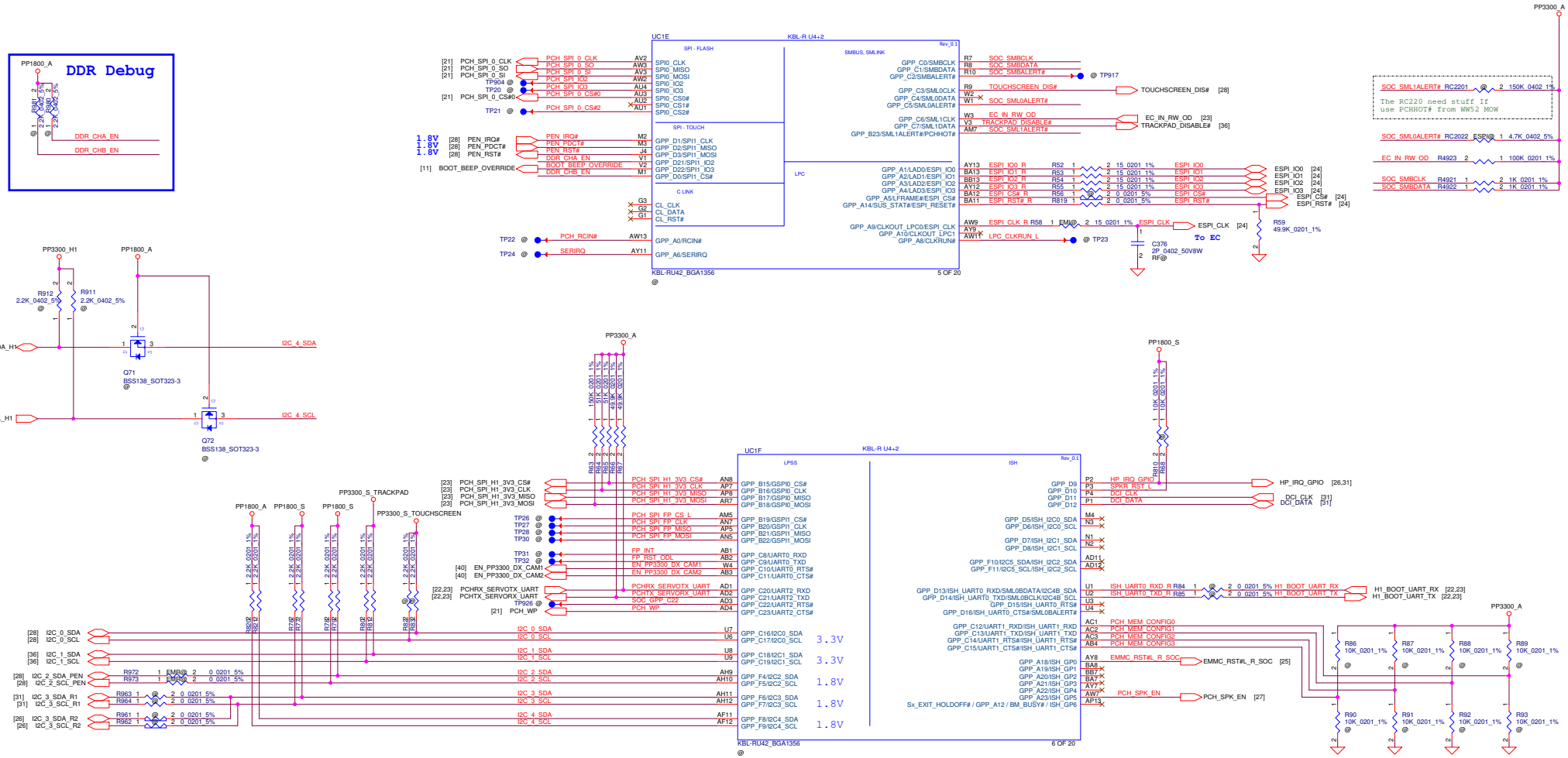

I2C Bus	Functon	Bus Voltage	Module Voltage
I2C_0	Touch Screen	3.3V	3.3V
I2C_1	Track Pad	3.3V	3.3V
I2C_2	PEN	1.8V	1.8V
I2C_3	HP AMP	1.8V	1.8V
I2C_4	N/A	1.8V	N/A

PIN	FUNCTION	INTENT
GPP_B_23/SML1ALERTB#	IPD = EXI BOOT STALL BYPASS DISABLE PU = EXI BOOT STALL BYPASS ENABLED	DISABLE
GPP_B18/GSPI0_MOSI	IPD = DISABLE NO REBOOT MODE PU = ENABLE NO REBOOT MODE	DISABLE
GPP_C2/SMBALERT#	IPD = DISABLE TLS CONFIDENTIALITY PU = ENABLE TLS CONFIDENTIALITY	DISABLE
GPP_B22/GSPI1_MOSI	IPD = BOOT FROM SPI PU = BOOT FROM LPC	SPI
GPP_C5/SML0ALERT#	IPD = LPC IS SELECTED FOR EC PU = ESPI IS SELECTED FOR EC	ESPI

STRAPS ON THIS PAGE

PIN	FUNCTION	INTENT
GPP_E19/DDPB_CTRLDATA	IPD = DO NOT DETECT PORT B PU = DETECT PORT B	DETECT PORT B
GPP_E21/DDPC_CTRLDATA	IPD = DO NOT DETECT PORT C PU = DETECT PORT C	DETECT PORT C

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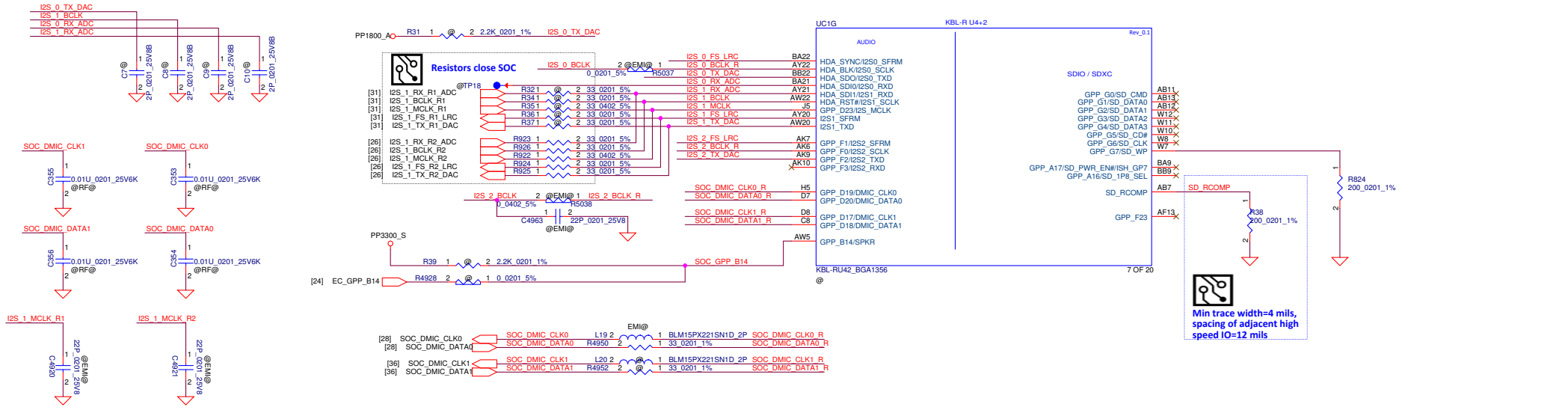
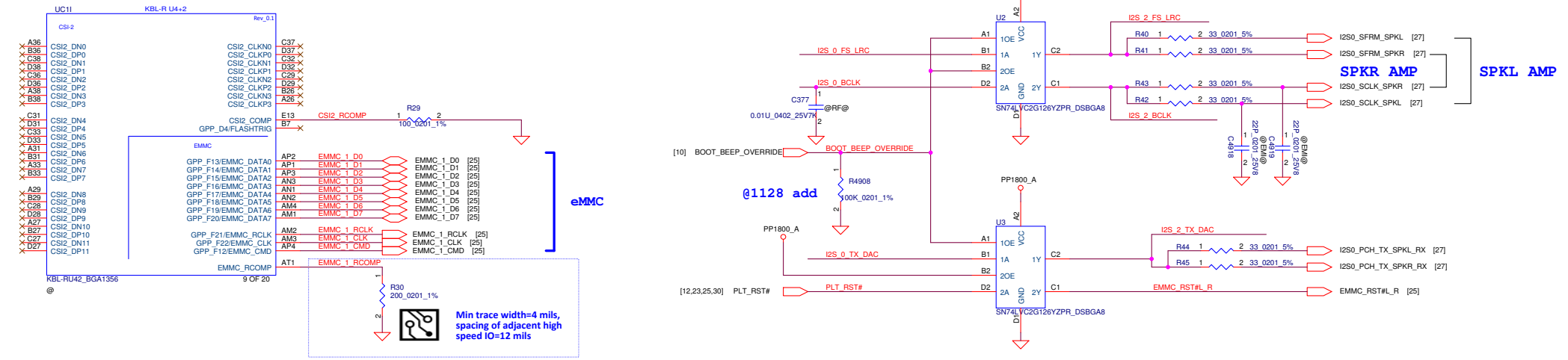


STRAPS ON THIS PAGE

PIN	FUNCTION	INTENT
PCH_BUZZER	IPD = DISABLE TOP SWAP OVERRIDE PU = ENABLE TOP SWAP OVERRIDE	DISABLE
HDA_SDO/I2S_TXD0	IPD = ENABLE DESCRIPTOR SECURITY PU = DISABLE DESCRIPTOR SECURITY	ENABLE



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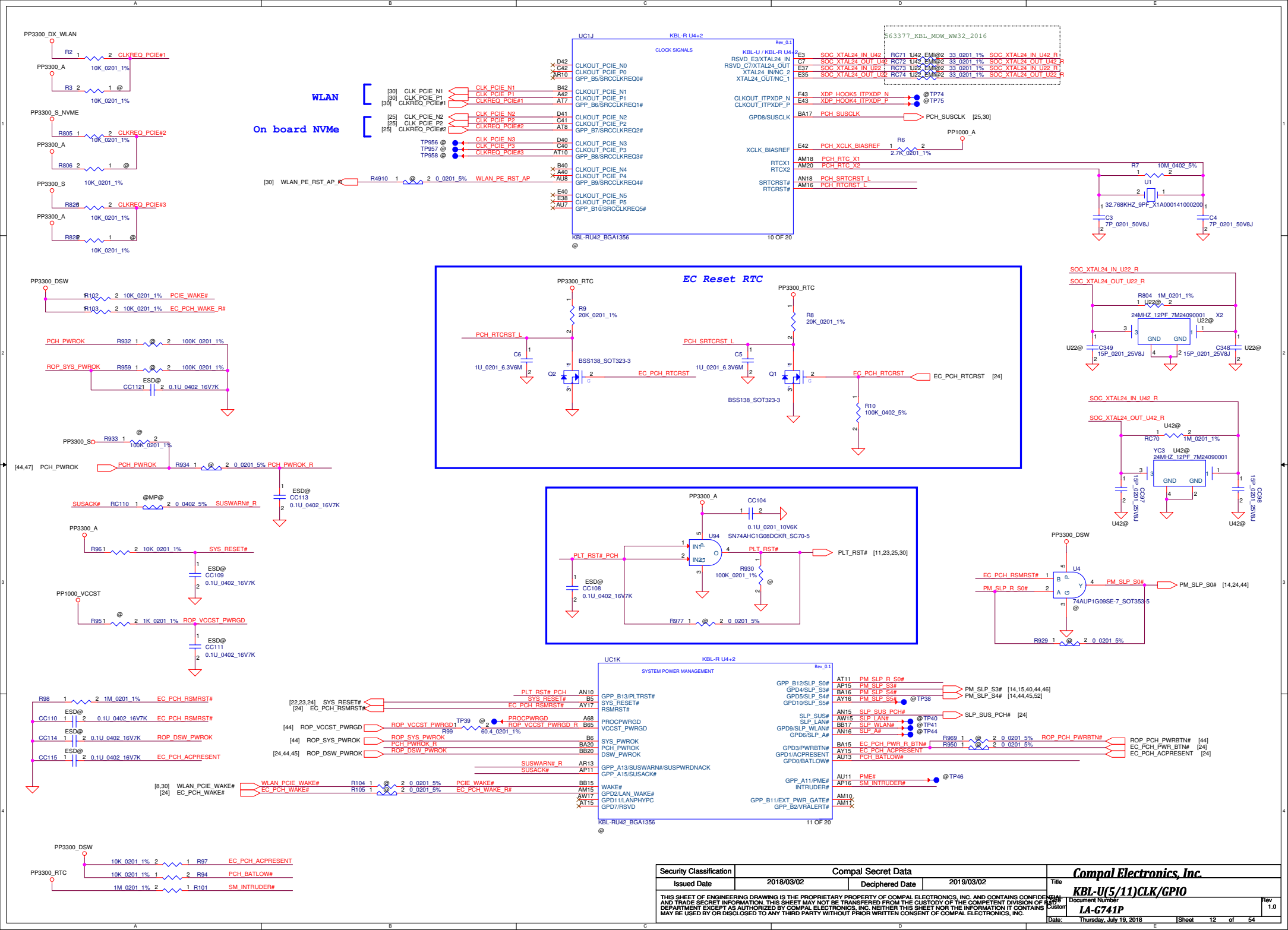

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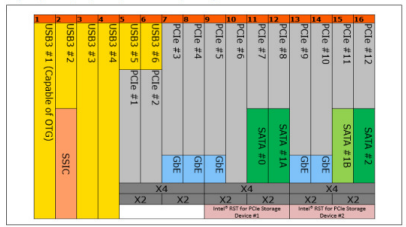
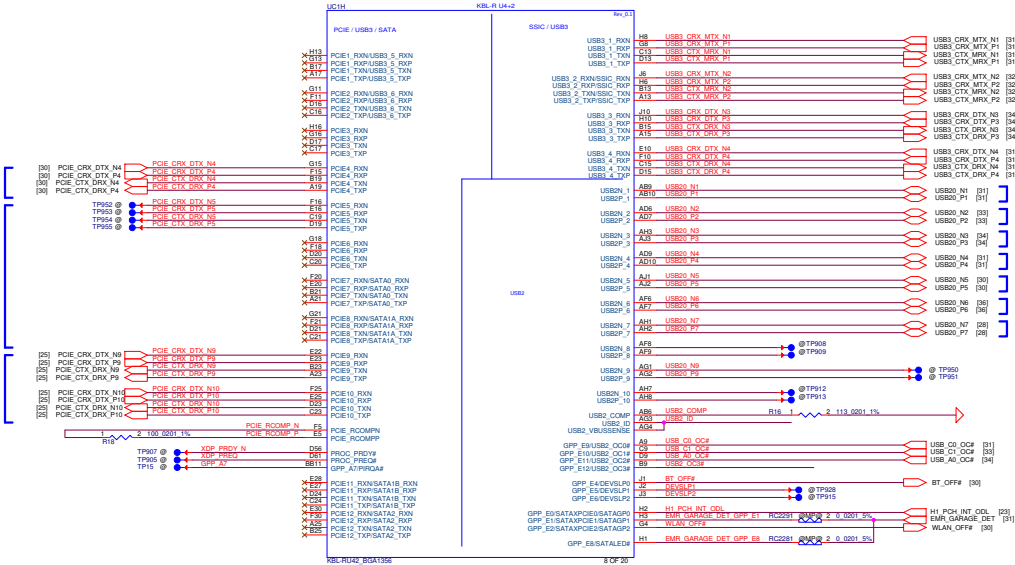


The 16 HSIO lanes on KBL R U PCH-LP supports the following configurations:

1. Up to 12 PCIe* lanes (multiplexed with USB 3.0 lanes, SATA lanes)
   - Only a maximum of 6 PCIe* Root Ports (or devices) can be enabled at any time
   - PCIe* Lanes 1-4, 5-8, and 9-12 each can be individually configured as 4x1, 2x2, 1x2+2x1, 2x1+1x2, or 1x4
2. Up to 3 SATA lanes (multiplexed with PCIe* lanes)
   - SATA lane 1 has the flexibility to be mapped to either PCIe* lane 8 or 11
3. Up to 6 USB 3.0 lanes (multiplexed with PCIe* lanes)
   - On-the-Go (OTG) capability is available on USB 3.0 lane 1
   - One SSIC x1 lane is multiplexed with USB 3.0 lane 2
4. One GbE device
   - GbE can be mapped into one of the PCIe* lanes 3-5 and 9-10
   - When GbE is enabled, there can be at most up to 5 PCIe* Root Ports (or devices) enabled
5. Up to 2 Intel® RST for PCIe* Storage Devices
   - Each device can be x2 or x4 and can be implemented on either PCIe* lanes 5-8 or 9 - 12
6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.

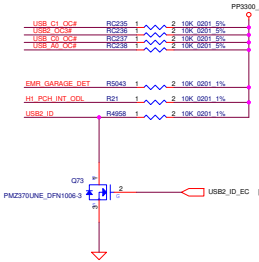
Table 1-3. PCH HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U / Base-U with iHDCP	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U / Premium-U with iHDCP	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y / Premium-Y with iHDCP	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A



Follow 561280_KBL UY PDG Rev1_0.pdf & 561280_KBL UY PDG Schematic Checklist Rev1_0.docx

If OTG is not implemented on the platform, then USB2_ID and USB2_VBUSSENSE should both be connected to ground.



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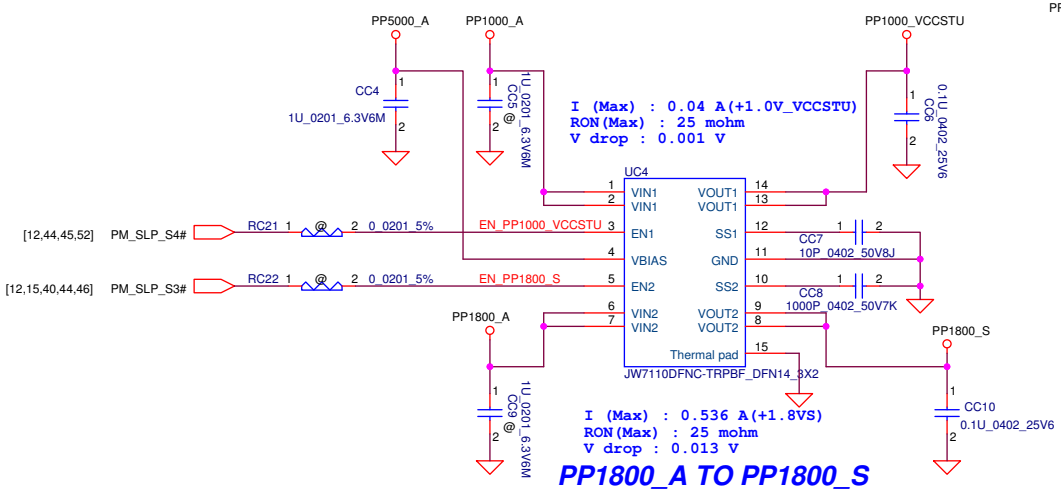
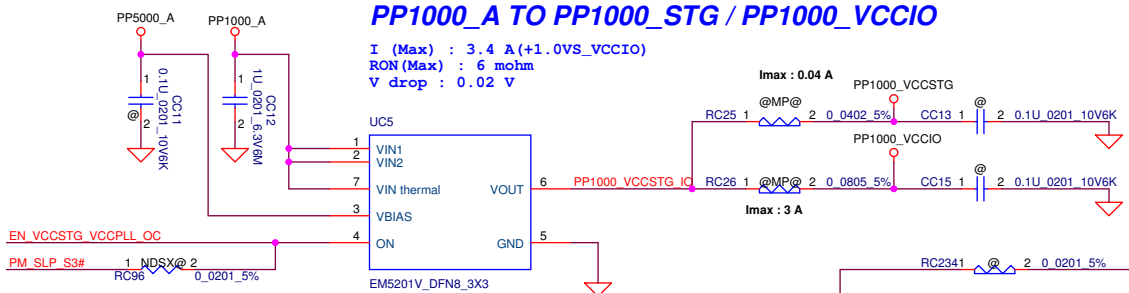
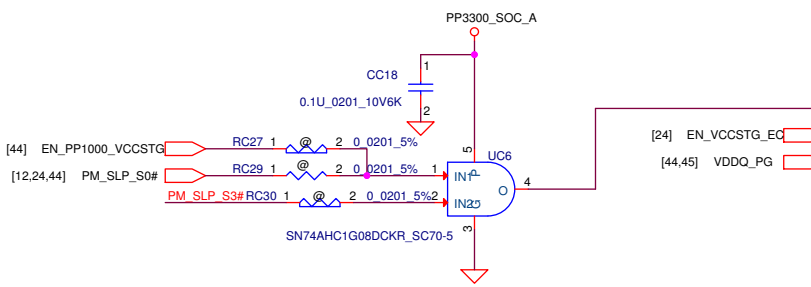
PP1000_A TO PP1000_VCCSTU

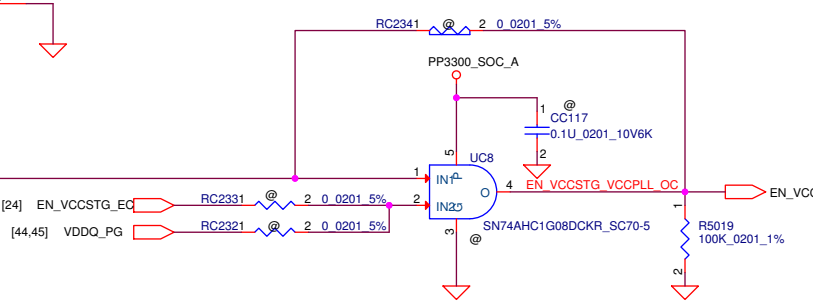


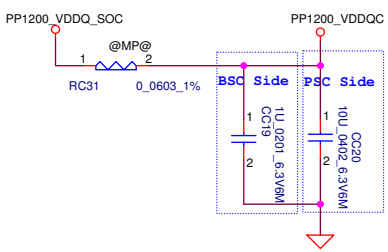
PP1800_A TO PP1800_S

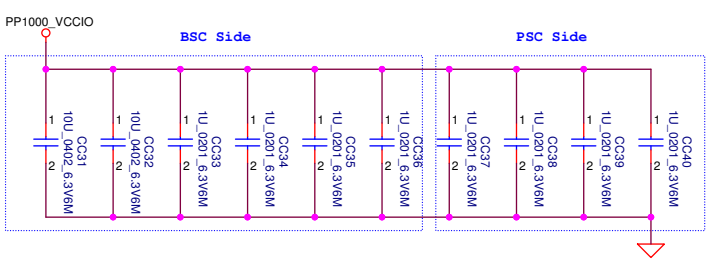
PP1000_A TO PP1000_STG / PP1000_VCCIO

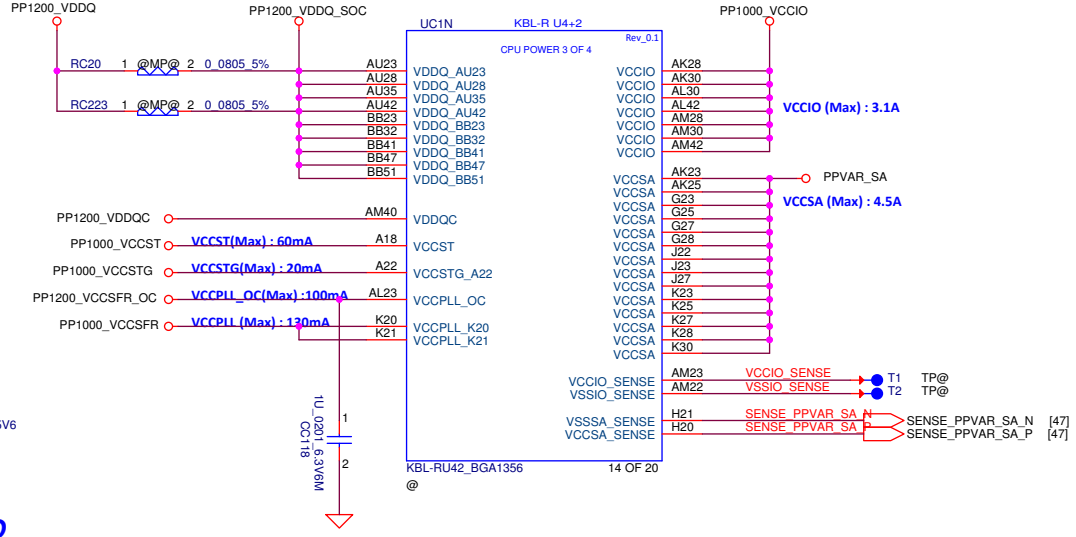


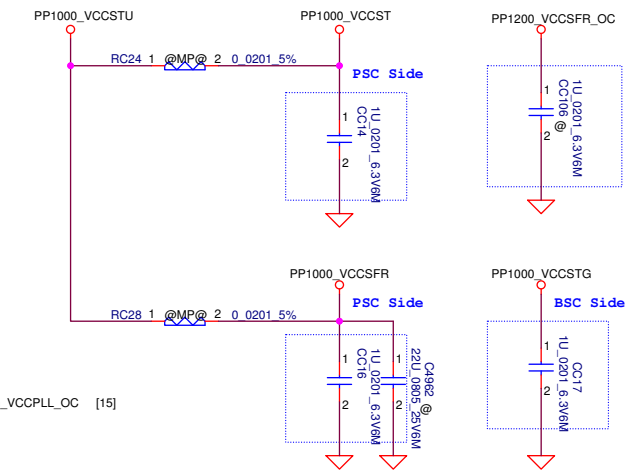


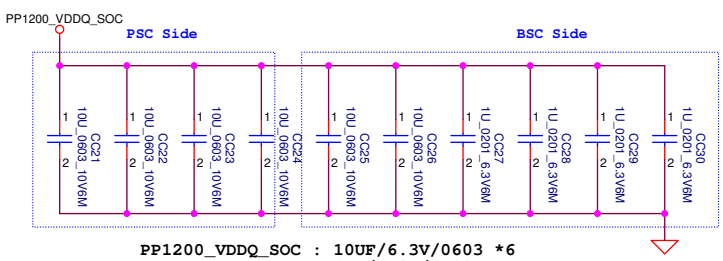












PP1200_VDDQ_SOC : 10UF/6.3V/0603 *6
1UF/6.3V/0402 * 4

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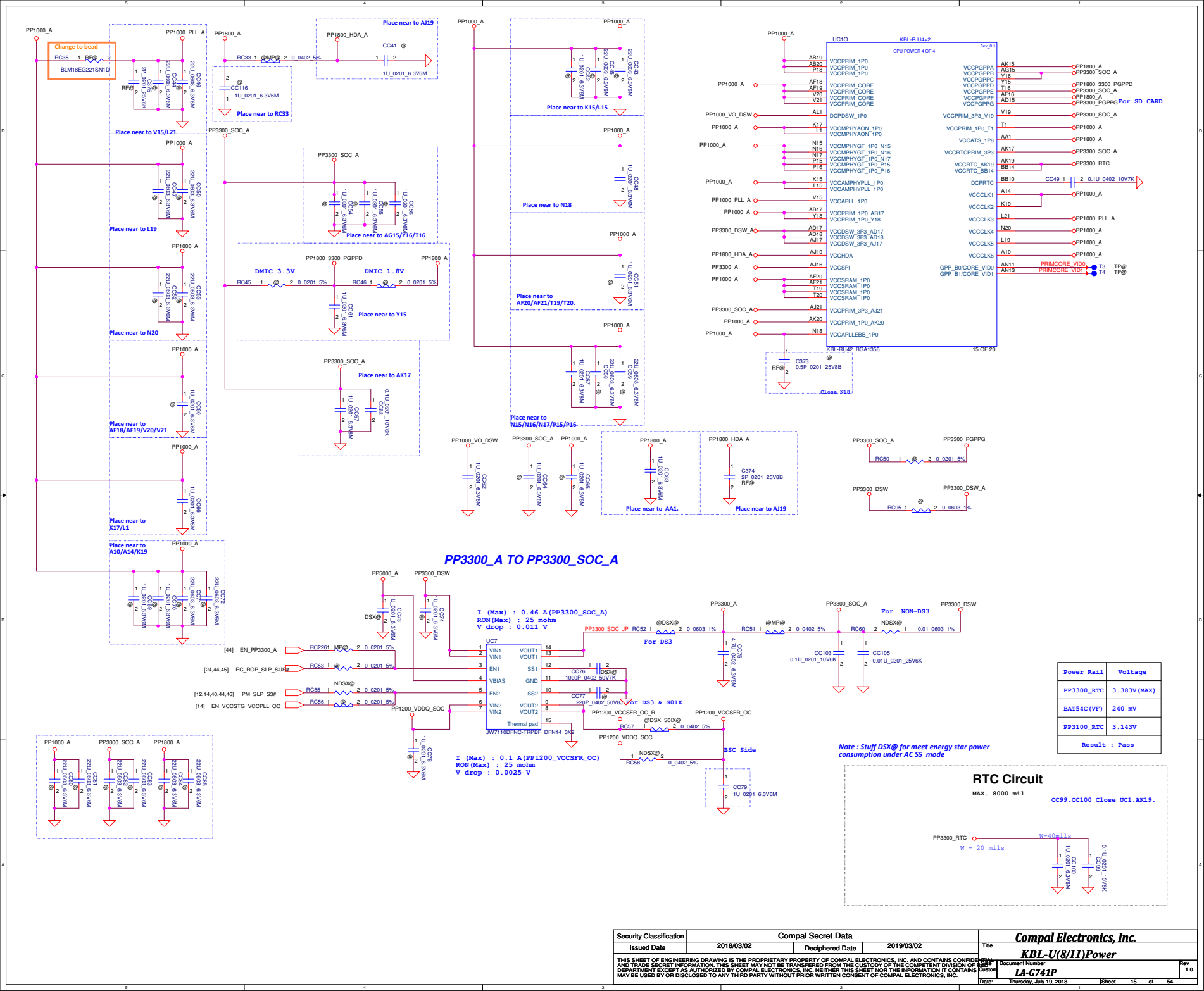
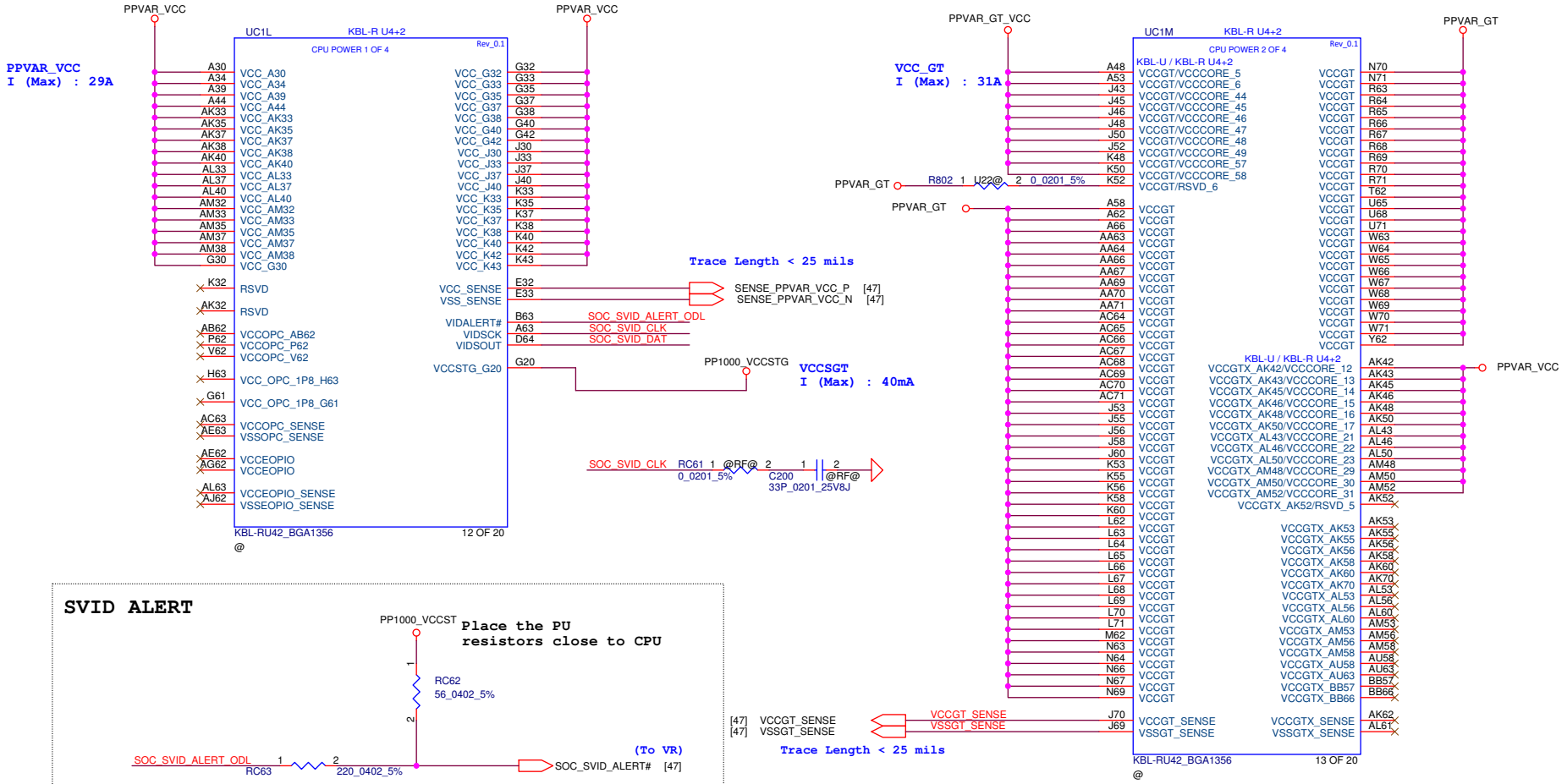

PP3300_A TO PP3300_SOC_A
Change to bead
RC35 1 RF@ 2
BLM18EG221SN1D
Place near to V15/L21
Place near to L19
Place near to N20
Place near to AF18/AF19/V20/V21
Place near to K17/L1
Place near to A10/A14/K19
Place near to RC33
Place near to AJ19
Place near to AG15/Y16/T16
DMIC 3.3V
DMIC 1.8V
Place near to Y15
Place near to AK17
Place near to K15/L15
Place near to N18
Place near to AF20/AF21/T19/T20.
Place near to N15/N16/N17/P15/P16
Place near to AA1.
Place near to AJ19
I (Max) : 0.46 A(PP3300_SOC_A)
RON(Max) : 25 mohm
V drop : 0.011 V
For DS3
For NON-DS3
For DS3 & S0IX
I (Max) : 0.1 A(PP1200_VCCSFR_OC)
RON(Max) : 25 mohm
V drop : 0.0025 V
BSC Side
Note : Stuff DSX@ for meet energy star power consumption under AC S5 mode
RTC Circuit
MAX. 8000 mil
CC99.CC100 Close UC1.AK19.
W=40mils
W = 20 mils
For SD CARD
Close N18
Power Rail | Voltage
PP3300_RTC | 3.383V(MAX)
BAT54C(VF) | 240 mV
PP3100_RTC | 3.143V
Result : Pass
Security Classification | Compal Secret Data
Issued Date | 2018/03/02 | Deciphered Date | 2019/03/02
Compal Electronics, Inc.
KBL-U(8/11)Power
Document Number LA-G741P
Rev 1.0
Date: Thursday, July 19, 2018 Sheet 15 of 54



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: KBL-U(9/11)Power,SVID

Size	Document Number	Rev
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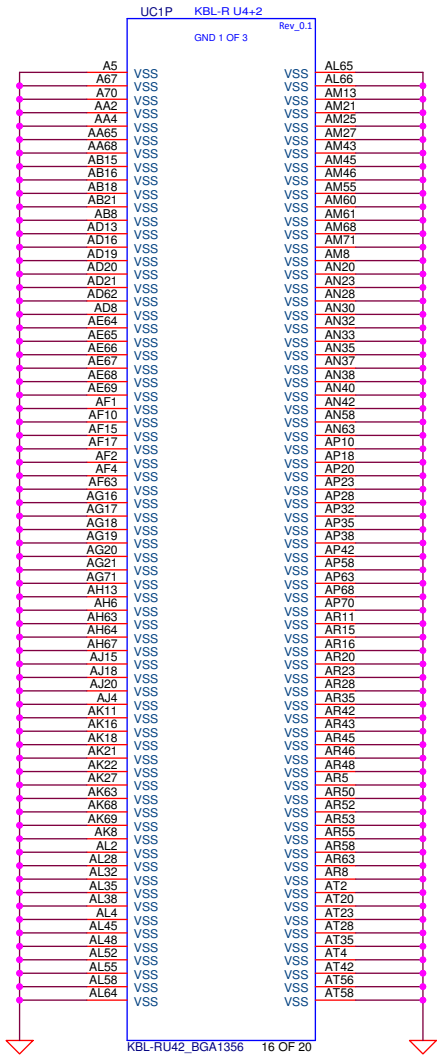

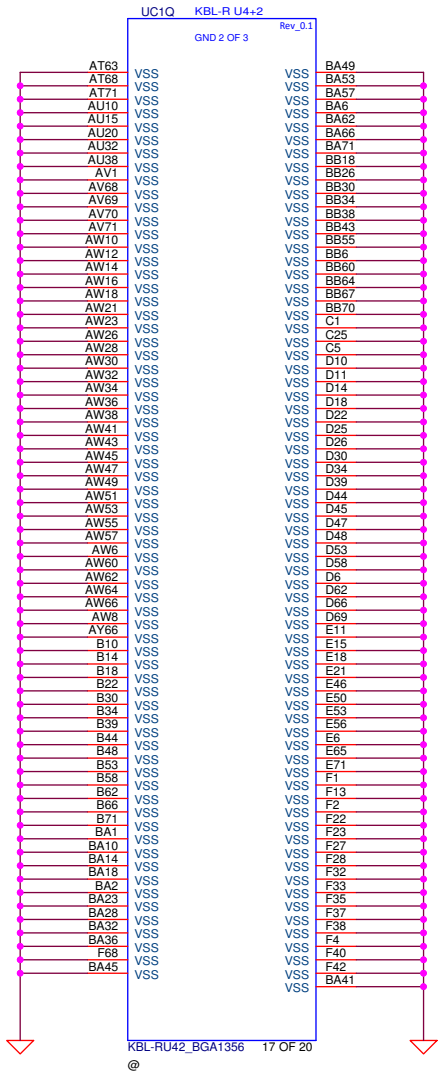

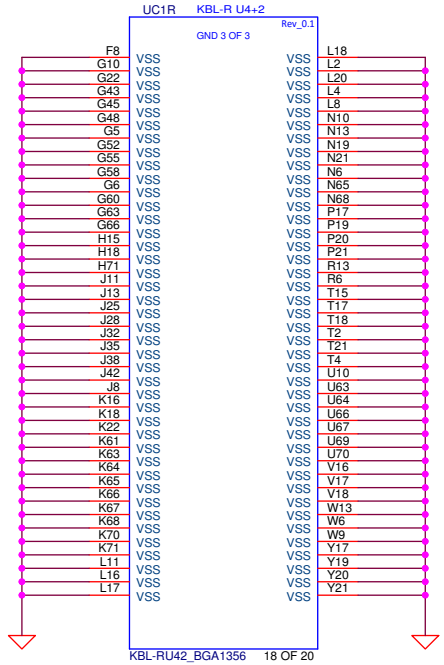

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Compal Electronics, Inc.

Title: **KBL-U(10/11)GND**

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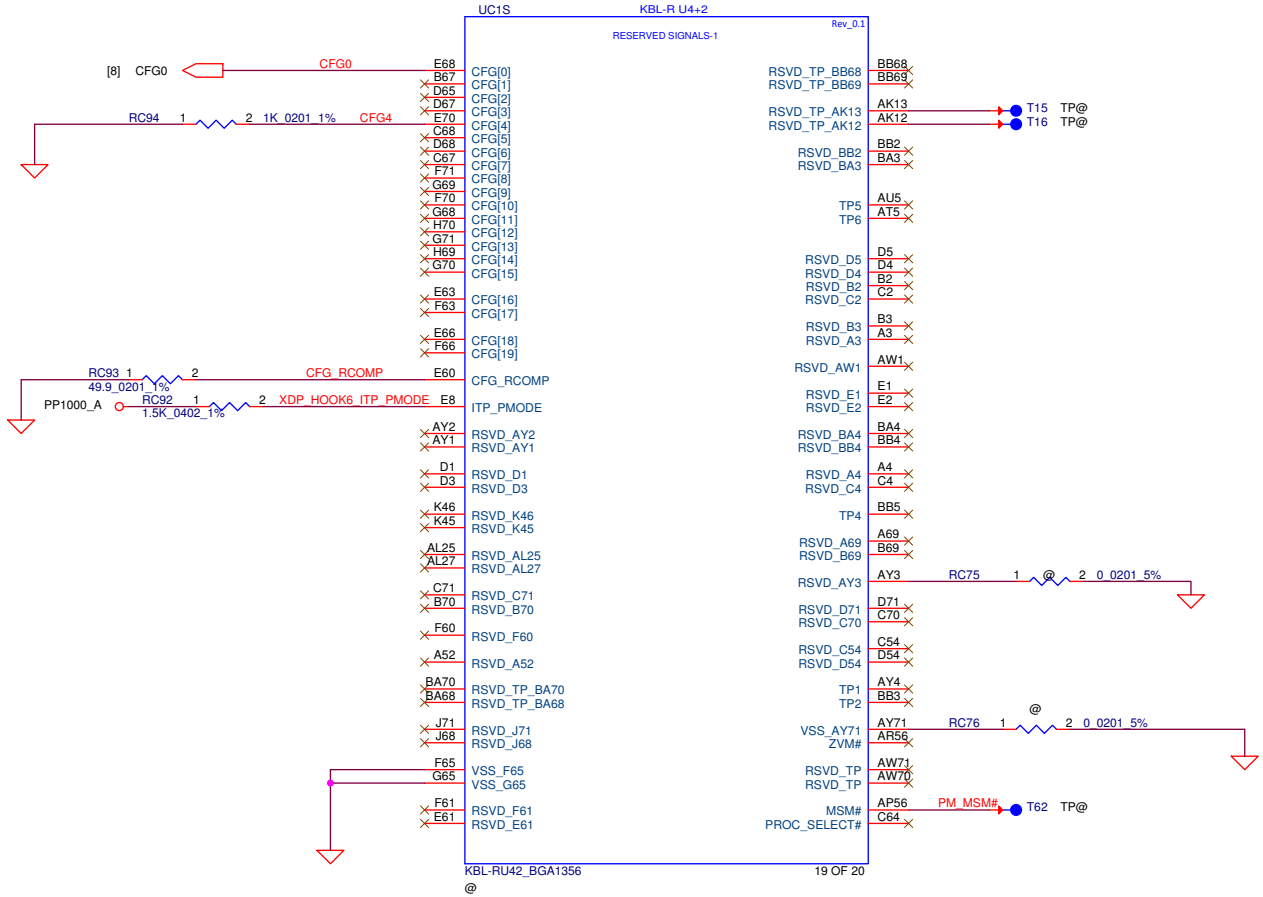
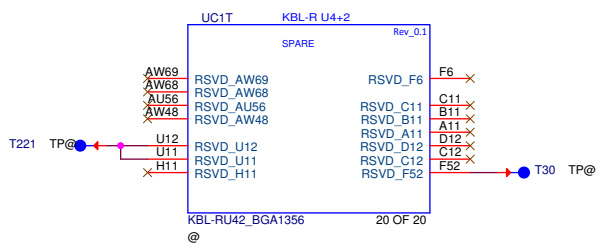
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port





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Compal Electronics, Inc.

Title: KBL-U(11/11)RSVD

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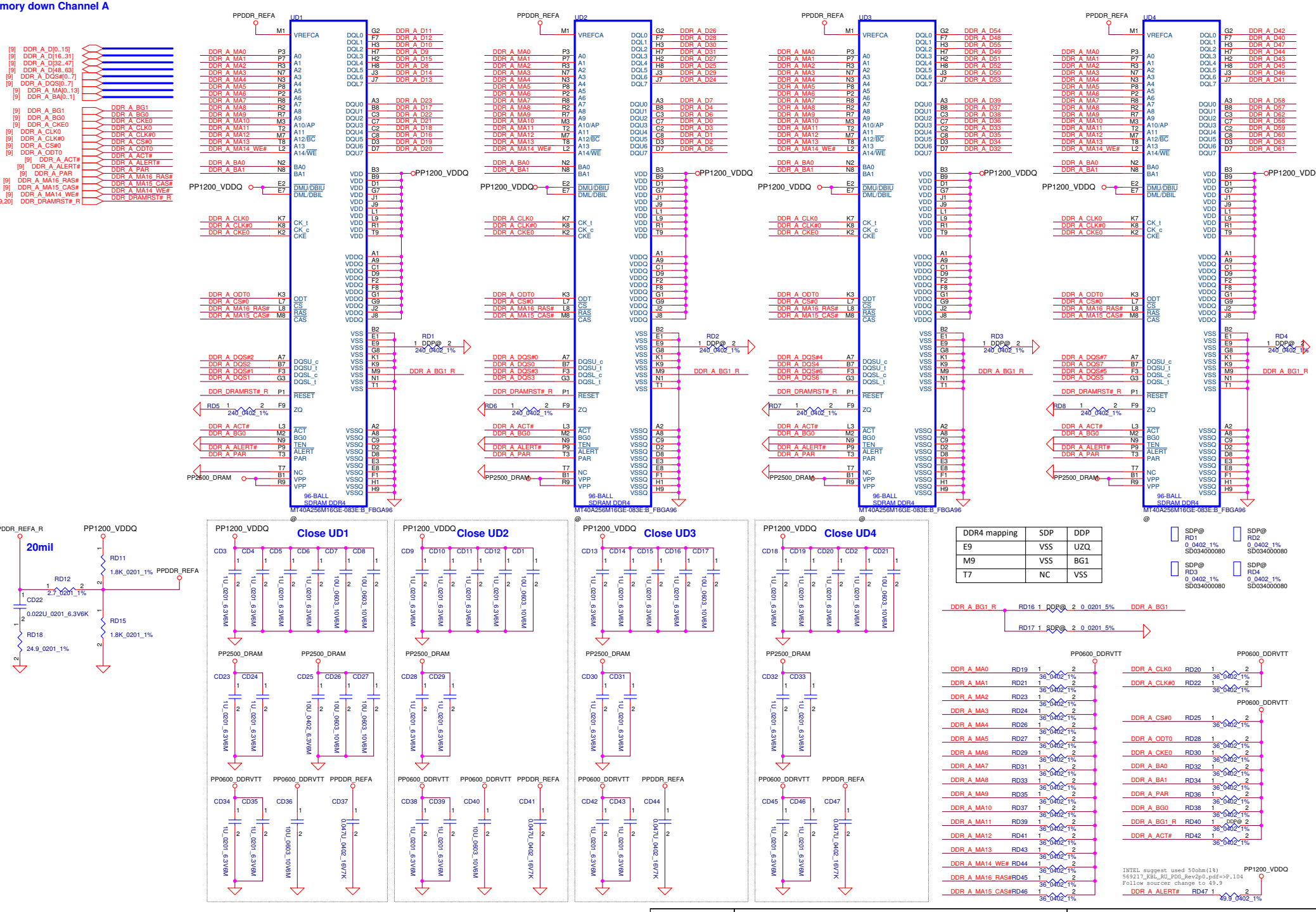
Memory down Channel A



DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS

SDP@ RD1 0_0402_1% SD034000080
SDP@ RD2 0_0402_1% SD034000080
SDP@ RD3 0_0402_1% SD034000080
SDP@ RD4 0_0402_1% SD034000080

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Issued Date	2018/03/02	Deciphered Date	2019/03/02

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Compal Electronics, Inc.

Title: DDR4 CHA Memory Down I

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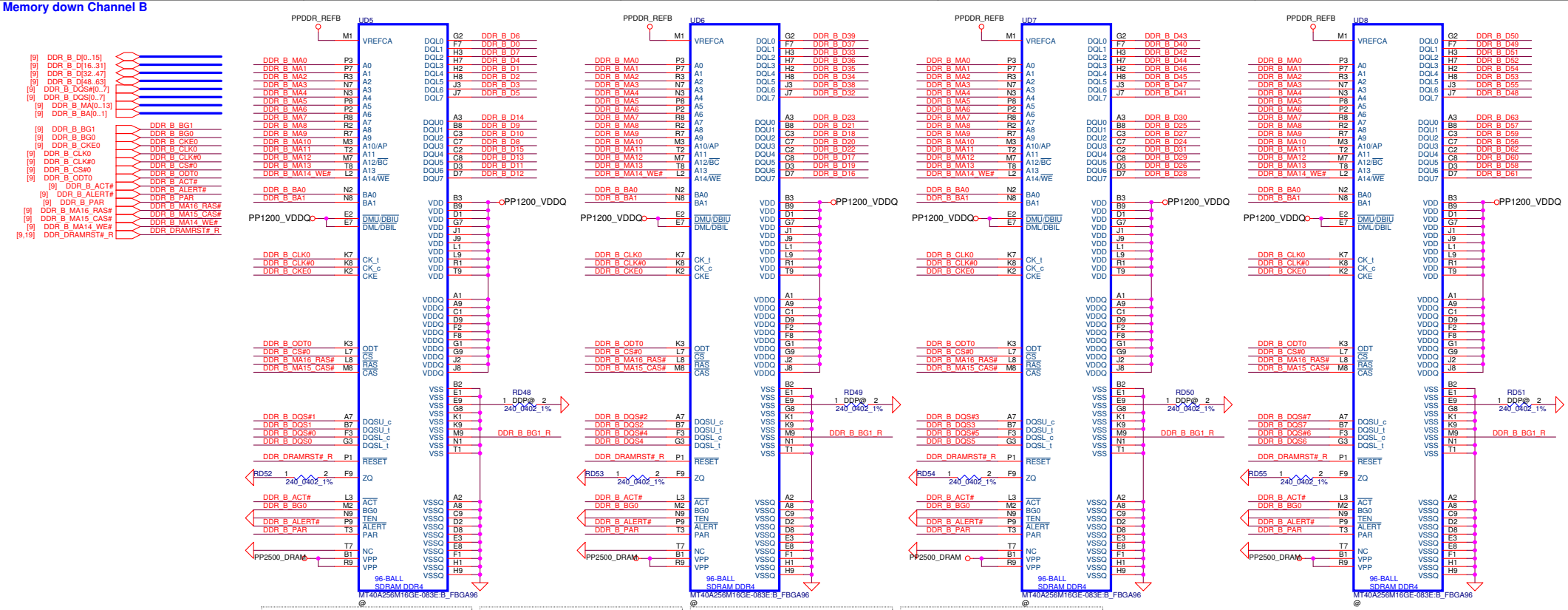
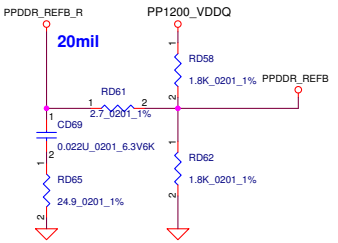
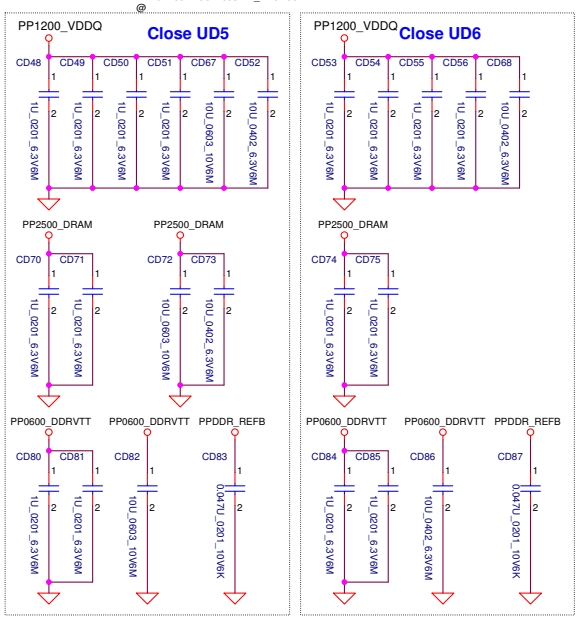
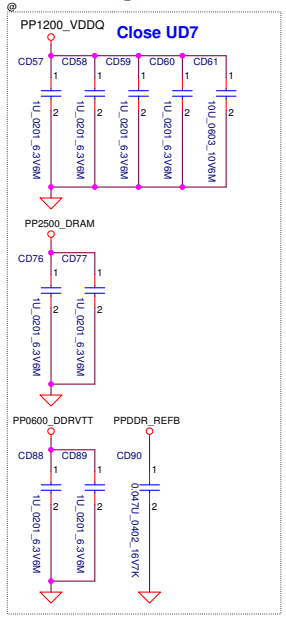
Date: Thursday, July 19, 2018 | Sheet 19 of 54

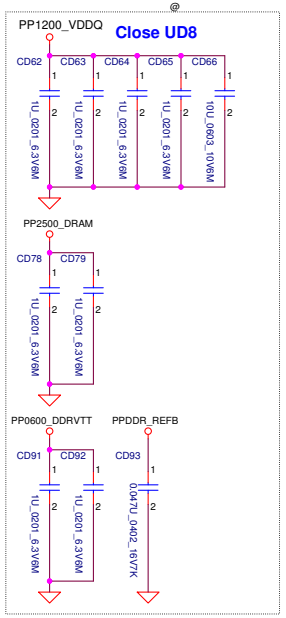
Memory down Channel B





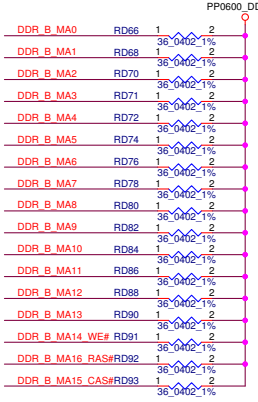


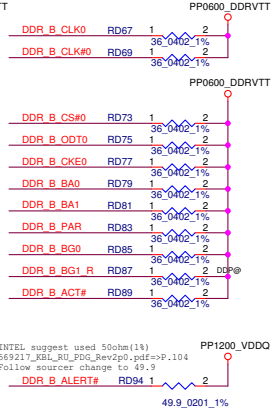




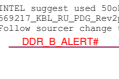
DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS

SDP@ RD48 0_0402_1% SD034000080
SDP@ RD49 0_0402_1% SD034000080
SDP@ RD50 0_0402_1% SD034000080
SDP@ RD51 0_0402_1% SD034000080





INTEL suggest used 50ohm(1%)
569217_KBL_RU_PDG_Rev2p0.pdf=>P.104
Follow sourcer change to 49.9



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Title	Compal Electronics, Inc.
	DDR4_CHA_Memory Down II
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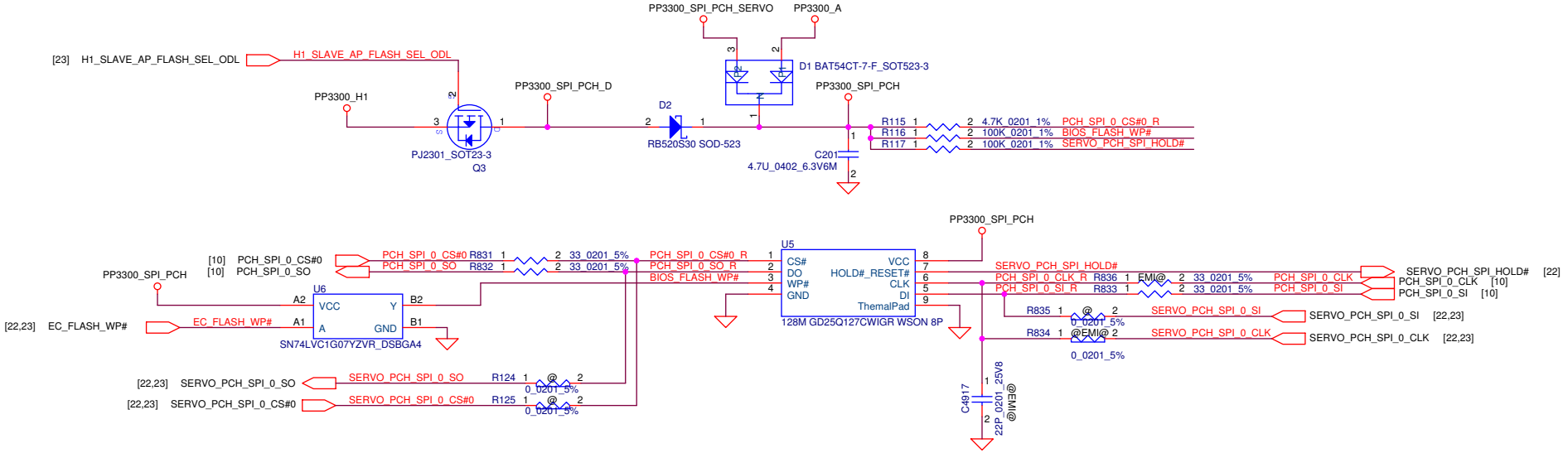
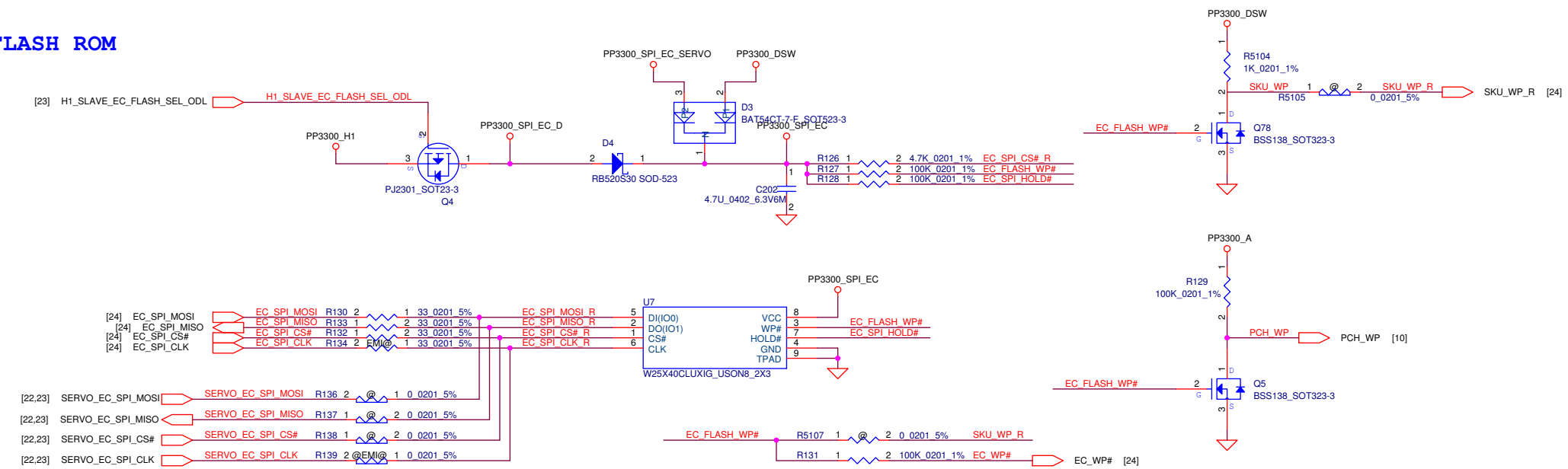
PCH SPI FLASH



EC FLASH ROM



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Compal Electronics, Inc.

Title: SPI EC ROM

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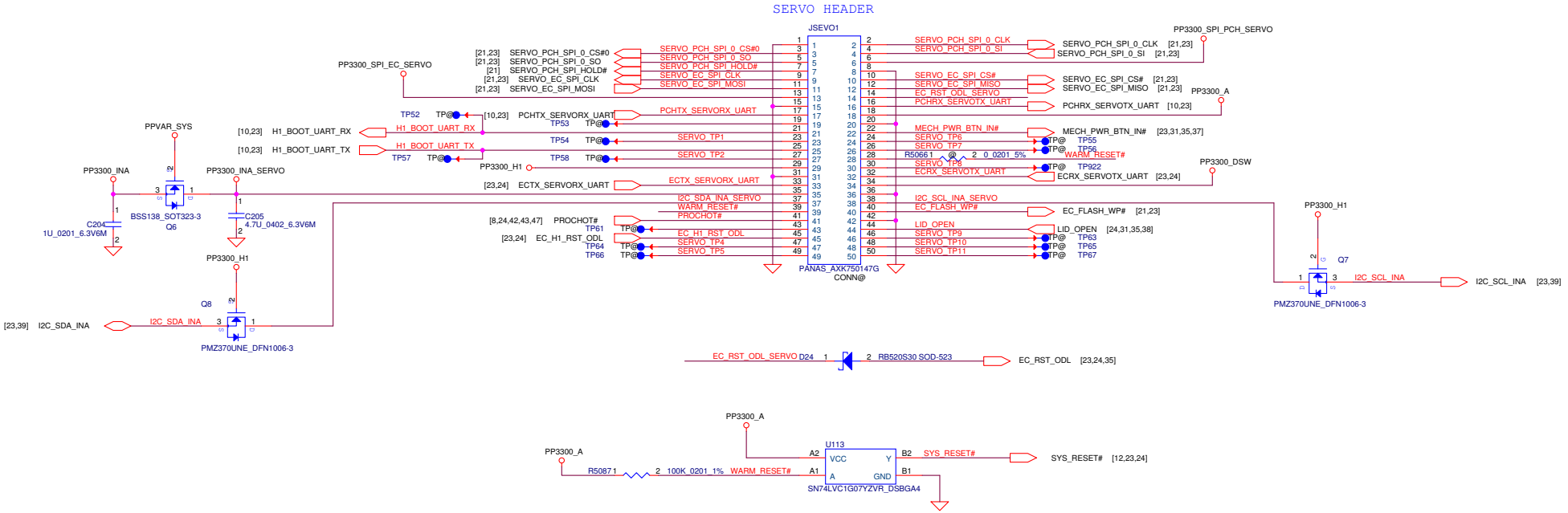

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Compal Electronics, Inc.			
Title: SERVO			
Size: Custom	Document Number: LA-G741P		Rev: 1.0
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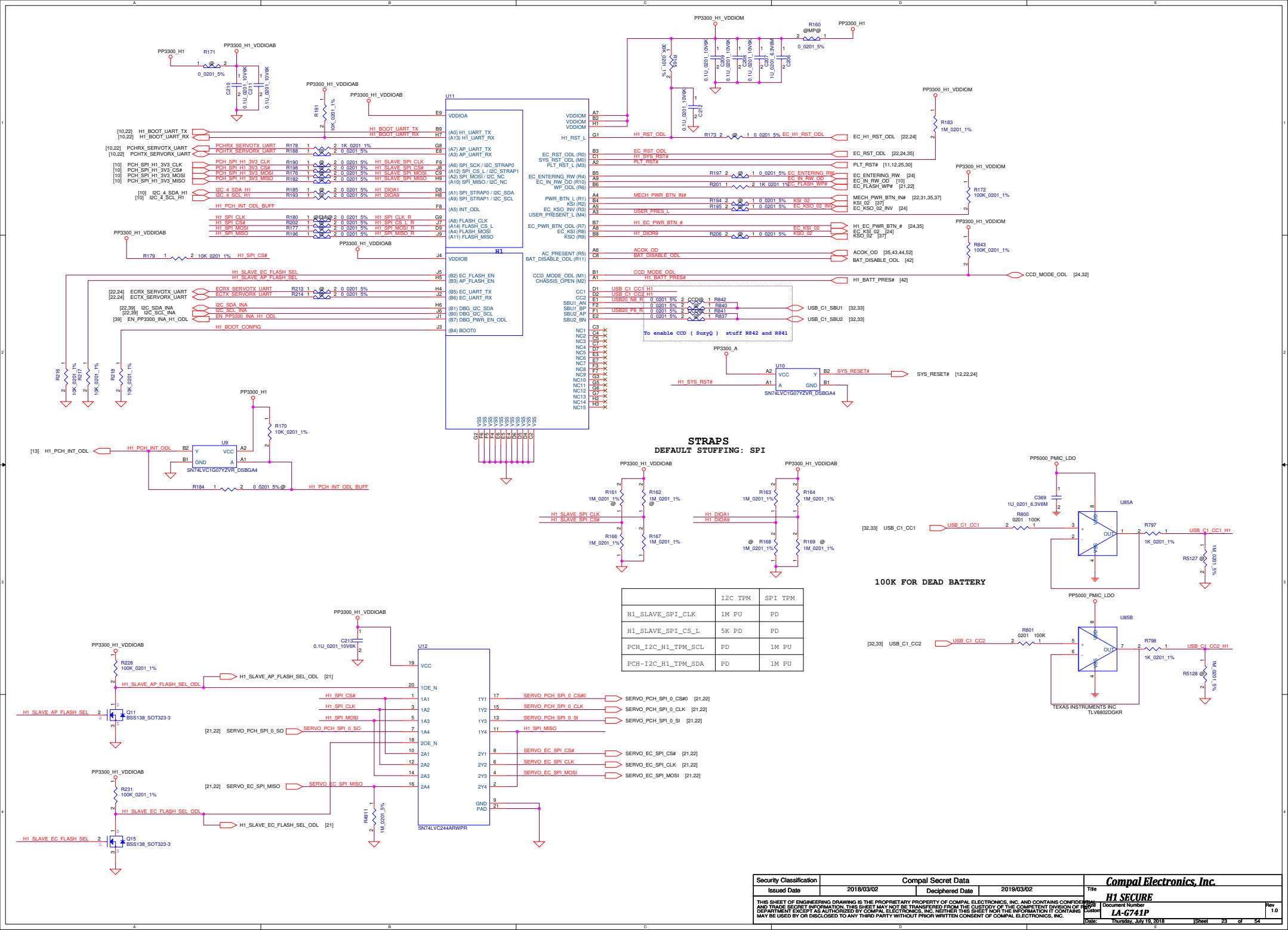

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Compal Electronics, Inc.

Title: H1 SECURE

Size: Custom | Document Number: LA-G741P | Rev: 1.0

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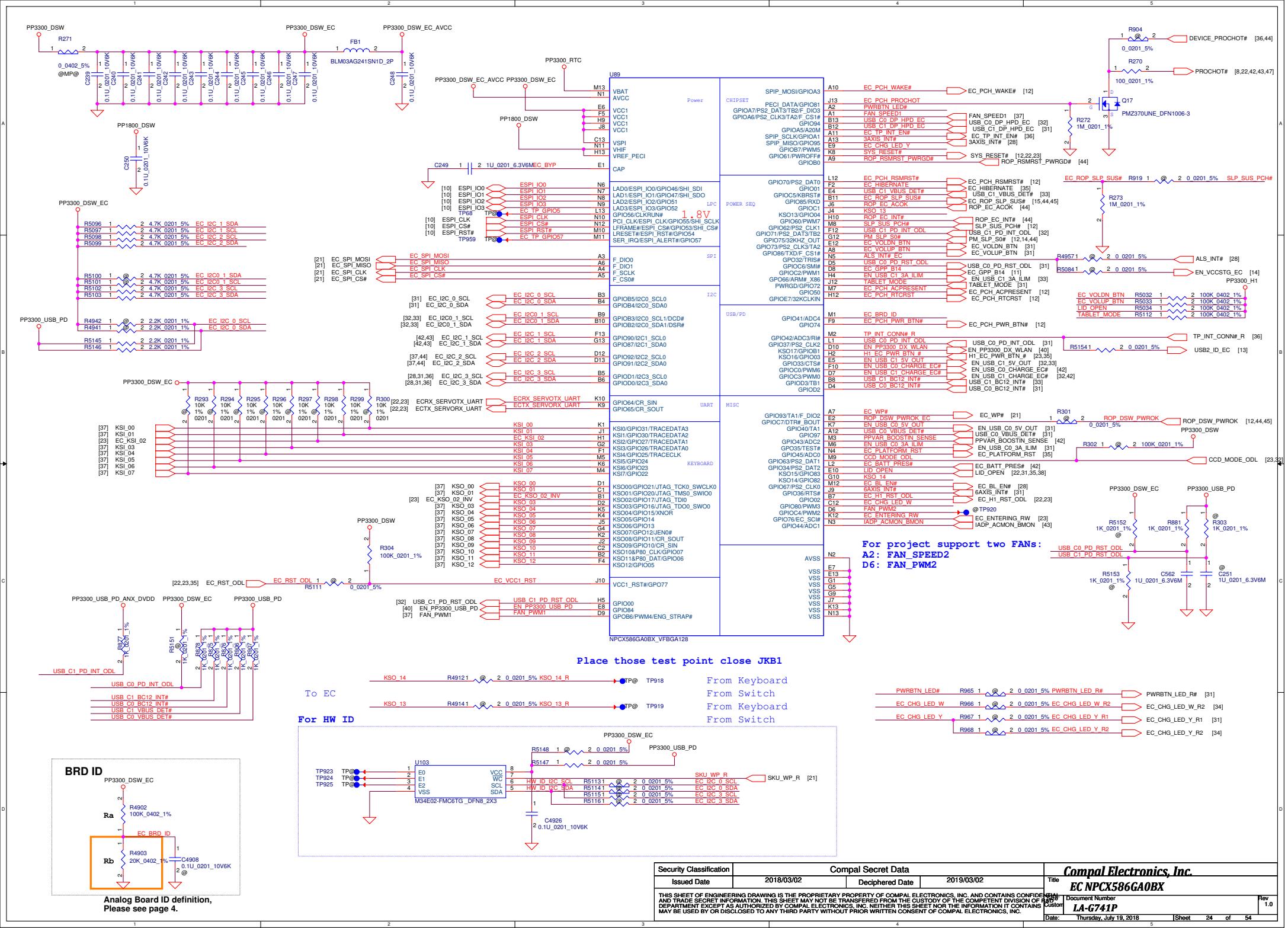
PP3300_DSW
PP3300_DSW_EC
PP3300_DSW_EC_AVCC
FB1
BLM03AG241SN1D_2P
PP1800_DSW
PP3300_RTC
U89
NPCX586GA0BX_VFBGA128
1.8V
PP3300_USB_PD
PP3300_H1
PP3300_USB_PD_ANX_DVDD
For project support two FANs:
A2: FAN_SPEED2
D6: FAN_PWM2
Place those test point close JKB1
To EC
For HW ID
From Keyboard
From Switch
From Keyboard
From Switch
BRD ID
Analog Board ID definition,
Please see page 4.
Compal Secret Data
2018/03/02
2019/03/02
Compal Electronics, Inc.
EC NPCX586GA0BX
LA-G741P
Thursday, July 19, 2018
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EMMC STORAGE

NVME STORAGE

U14C — FSVLMJC-128G_BGA_345P

U14D — FSVLMJC-128G_BGA_345P

U14A — FSVLMJC-128G_BGA_345P

U14B — FSVLMJC-128G_BGA_345P

PP1800_A

PP1800_S

PP1800_S_EMMC

PP3300_A

PP3300_S

PP3300_S_EMMC

PP1800_S_NVME

PP3300_S_NVME

PP1200_S_NVME

R4929 1 @ 2 0_0603_5%

R913 1 @EMMC@ 2 0_0603_1%

R4930 1 @ 2 0_0603_5%

R955 1 @EMMC@ 2 0_0603_1%

EMMC_1_D4 R5088 1 2 20K_0201_1%
EMMC_1_D3 R5089 1 2 20K_0201_1%
EMMC_1_D0 R5090 1 2 20K_0201_1%
EMMC_1_D1 R5091 1 2 20K_0201_1%
EMMC_1_D2 R5092 1 2 20K_0201_1%
EMMC_1_D6 R5093 1 2 20K_0201_1%
EMMC_1_D7 R5094 1 2 20K_0201_1%
EMMC_1_D5 R5095 1 2 20K_0201_1%

R824 1 EMMC@ 2 20K_0201_1%

EMMC_VDDI_BYP

C71 1U_0201_6.3V6M EMMC@

C72 4.7U_0402_10V6M EMMC@
C77 0.1U_0201_10V6K EMMC@
C73 4.7U_0402_10V6M EMMC@
C78 0.1U_0201_10V6K EMMC@

C68 2.2U_0402_10V6M NVME@
C74 0.1U_0201_10V6K NVME@
C79 0.1U_0201_10V6K NVME@
C69 2.2U_0402_10V6M NVME@
C75 0.1U_0201_10V6K NVME@
C80 0.1U_0201_10V6K NVME@
C70 2.2U_0402_10V6M NVME@
C76 0.1U_0201_10V6K NVME@
C81 0.1U_0201_10V6K NVME@

C4914 15P_0201_25V8J @EMC@
C4915 15P_0201_25V8J @EMC@

R857 1 20K_0201_1% EMMC@ 2
R821 1 20K_0201_1% EMMC@ 2
R903 1 100K_0201_1% EMMC@ 2

EMMC_RST#L_R

D222 1 RB751S-40 PLT_RST#

PLT_RST# [11,12,23,30]

R4931 1 @ 2 0_0201_5% EMMC_RST#L_R_SOC

EMMC_RST#L_R_SOC [10]

EMMC_RST#L_R [11]

EMMC_CLK_R R863 1 EMC@ 2 15_0201_1%
EMMC_CMD_R R866 @EMMC@ 2 0_0201_5%
EMMC_T_RCLK_R R920 1 EMC@ 2 15_0201_1%

EMMC_DAT0_R R854 @EMMC@ 2 0_0201_5%
EMMC_DAT1_R R855 @EMMC@ 2 0_0201_5%
EMMC_DAT2_R R849 @EMMC@ 2 0_0201_5%
EMMC_DAT3_R R848 @EMMC@ 2 0_0201_5%
EMMC_DAT4_R R860 @EMMC@ 2 0_0201_5%
EMMC_DAT5_R R853 @EMMC@ 2 0_0201_5%
EMMC_DAT6_R R856 @EMMC@ 2 0_0201_5%
EMMC_DAT7_R R862 @EMMC@ 2 0_0201_5%

EMMC_1_D0 [11]
EMMC_1_D1 [11]
EMMC_1_D2 [11]
EMMC_1_D3 [11]
EMMC_1_D4 [11]
EMMC_1_D5 [11]
EMMC_1_D6 [11]
EMMC_1_D7 [11]
EMMC_1_CLK [11]
EMMC_1_CMD [11]
EMMC_1_RCLK [11]

PCIE_CTX_C_DRX_P9 NVME@ C563 1 2 0.22U_0201_6.3V6K PCIE_CTX_DRX_P9
PCIE_CTX_C_DRX_N9 NVME@ C568 1 2 0.22U_0201_6.3V6K PCIE_CTX_DRX_N9
PCIE_CTX_C_DTX_P9 NVME@ C569 1 2 0.22U_0201_6.3V6K PCIE_CRX_DTX_P9
PCIE_CRX_C_DTX_N9 NVME@ C570 1 2 0.22U_0201_6.3V6K PCIE_CRX_DTX_N9
PCIE_CTX_C_DRX_P10 NVME@ C571 1 2 0.22U_0201_6.3V6K PCIE_CTX_DRX_P10
PCIE_CTX_C_DRX_N10 NVME@ C564 1 2 0.22U_0201_6.3V6K PCIE_CTX_DRX_N10
PCIE_CRX_C_DTX_P10 NVME@ C572 1 2 0.22U_0201_6.3V6K PCIE_CRX_DTX_P10
PCIE_CRX_C_DTX_N10 NVME@ C573 1 2 0.22U_0201_6.3V6K PCIE_CRX_DTX_N10

PCIE_CTX_DRX_P9 [13]
PCIE_CTX_DRX_N9 [13]
PCIE_CRX_DTX_P9 [13]
PCIE_CRX_DTX_N9 [13]
PCIE_CTX_DRX_P10 [13]
PCIE_CTX_DRX_N10 [13]
PCIE_CRX_DTX_P10 [13]
PCIE_CRX_DTX_N10 [13]

R901 1 100K_0201_1% NVME@ 2

D232 1 RB751S-40 PLT_RST#

R884 1 NVME@ 2 0_0201_5% PCH_SUSCLK

CLK_PCIE_P2 [12]
CLK_PCIE_N2 [12]
CLKREQ_PCIE#2 [12]
PCH_SUSCLK [12,30]

R889 1 49.9_0201_1% NVME@ 2
R888 1 49.9_0201_1% NVME@ 2

R5074 1 49.9_0201_1% @ 2
R5075 1 49.9_0201_1% @ 2
R5076 1 49.9_0201_1% @ 2

CLK_PCIE_P2
CLK_PCIE_N2
PLT_RST#
CLKREQ_PCIE#2
PCH_SUSCLK
NVME_PLT_RST_ODL
CLKREQ_PCIE#2
NVME_SUSCLK
NVME_24MHZ_XTAL_OUT
NVME_24MHZ_XTAL_IN

NVME_JTAG_TRST_N TP76
NVME_JTAG_TCK TP77
NVME_JTAG_TMS TP78
NVME_JTAG_TDI TP79
NVME_JTAG_TDO TP80
NVME_SMB_CLK TP81
NVME_SMB_DATA TP82
NVME_UART_RX TP83
NVME_UART_TX TP84

VDDI_NVME

VDDI_NVME is generated inside.

NVME_GPIO1
NVME_GPIO0 TP949
NVME_TEST_MODE

NVME_24MHZ_XTAL_IN
NVME_24MHZ_XTAL_OUT

R887 1 NVME@ 2 1M_0201_1%

R885 100_0201_1% NVME@
R886 0_0201_5% NVME@

Y3 40MHZ_8Y40000001 NVME@

C567 10P_0201_25V8 NVME@
C566 10P_0201_25V8 NVME@

C5000 10U_0603_10V8M NVME@
C4999 0.1U_0201_10V6K NVME@
C5001 1U_0201_6.3V6M NVME@

R5080 1 @NVME@ 10K_0201_5% NVME_GPIO0 R5077 1 NVME@ 2 1K_0201_5%
R5081 1 @NVME@ 10K_0201_5% NVME_GPIO1 R5078 1 NVME@ 2 1K_0201_5%
R5082 1 @NVME@ 10K_0201_5% NVME_TEST_MODE R5079 1 NVME@ 2 1K_0201_5%

Startup config: For FORESEE PCIe Gen3 BGA SSD P900		
NVME_GPIO0	0 Normal Mode	1 Firmware safe mode
NVME_GPIO1	0 ENABLES eFUSE DISABLES JTAG/UART	1 ENABLES JTAG/UART
NVME_TEST_MODE	0 Normal Mode	1 Test Mode

Security Classification	Compal Secret Data	
Issued Date	2018/03/02	Deciphered Date 2019/03/02

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Compal Electronics, Inc.

Title: eMMC / NVMe

Size: Custom | Document Number: LA-G741P | Rev: 1.0

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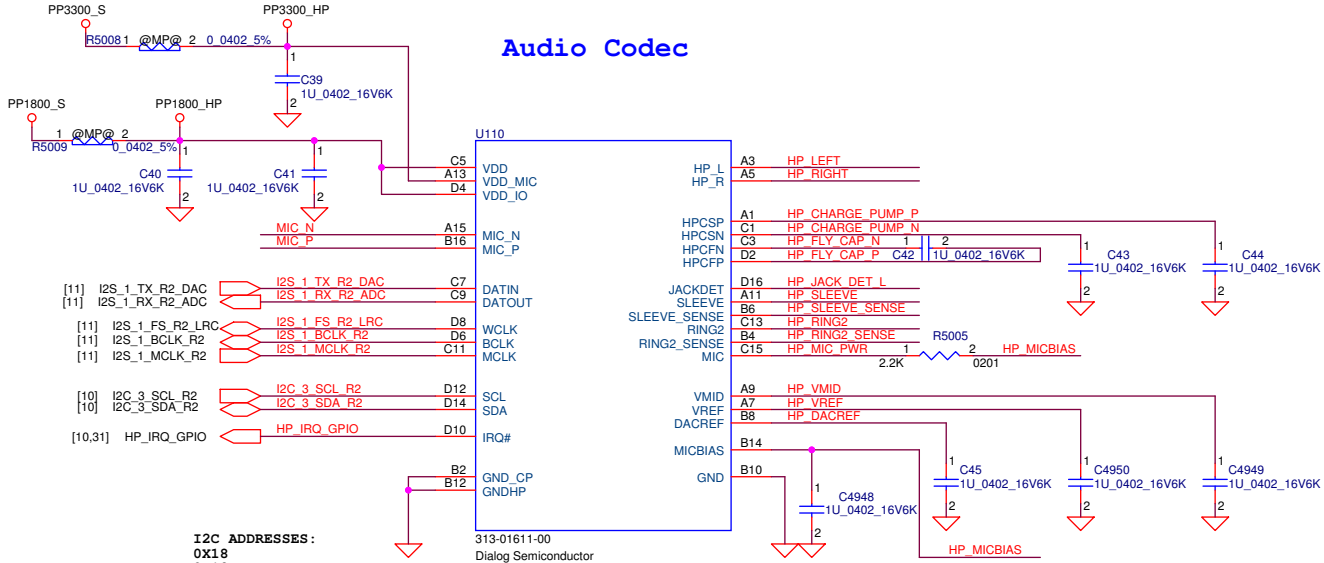
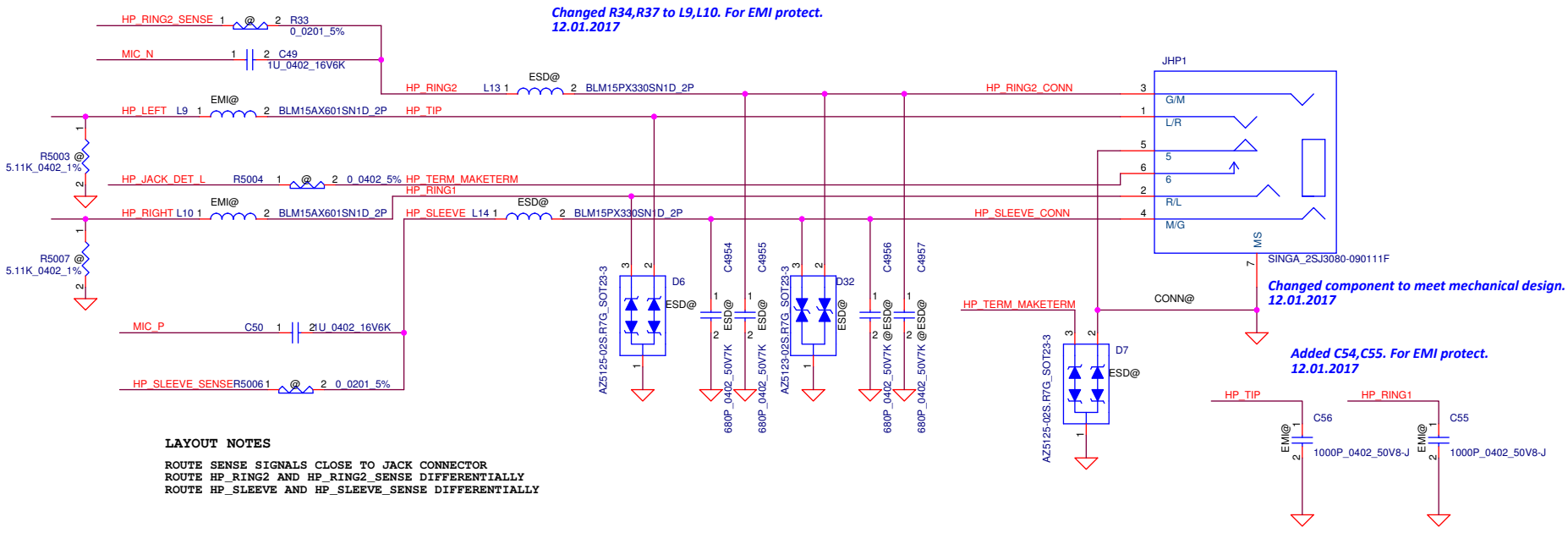
Audio Codec



I2C ADDRESSES:
0X18
0X19
0X1A (DEFAULT)
0X1B

Changed R34,R37 to L9,L10. For EMI protect.
12.01.2017



Changed component to meet mechanical design.
12.01.2017

Added C54,C55. For EMI protect.
12.01.2017

LAYOUT NOTES

ROUTE SENSE SIGNALS CLOSE TO JACK CONNECTOR
ROUTE HP_RING2 AND HP_RING2_SENSE DIFFERENTIALLY
ROUTE HP_SLEEVE AND HP_SLEEVE_SENSE DIFFERENTIALLY

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Issued Date	2018/03/02	Deciphered Date	2019/03/02

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Compal Electronics, Inc.

Title: **HP AMP DA7219-02VBA**

Size: Custom | Document Number: **LA-G741P** | Rev: 1.0

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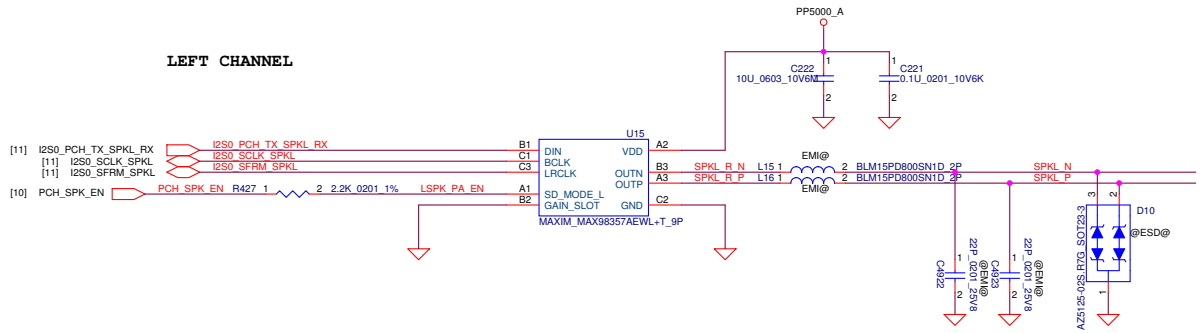
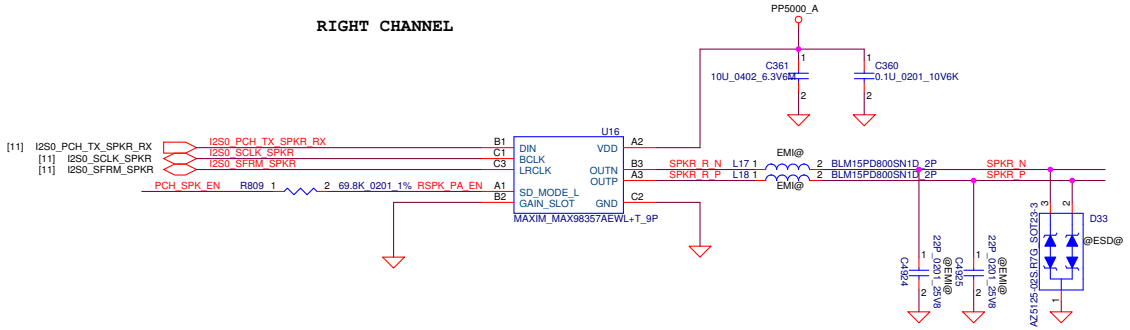
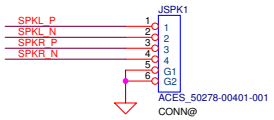
SPEAKER AMP





SPEAKER CONNECTOR



LAYOUT NOTES

SPKL_P, SPKL_N & SPKR_P, SPKR_N SHOULD BE CONNECTED AS CLOSE TO THE SPEAKER CONNECTOR AS POSSIBLE

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Issued Date	2018/03/02	Deciphered Date	2019/03/02

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Compal Electronics, Inc.

Title: SPEAKER AMP

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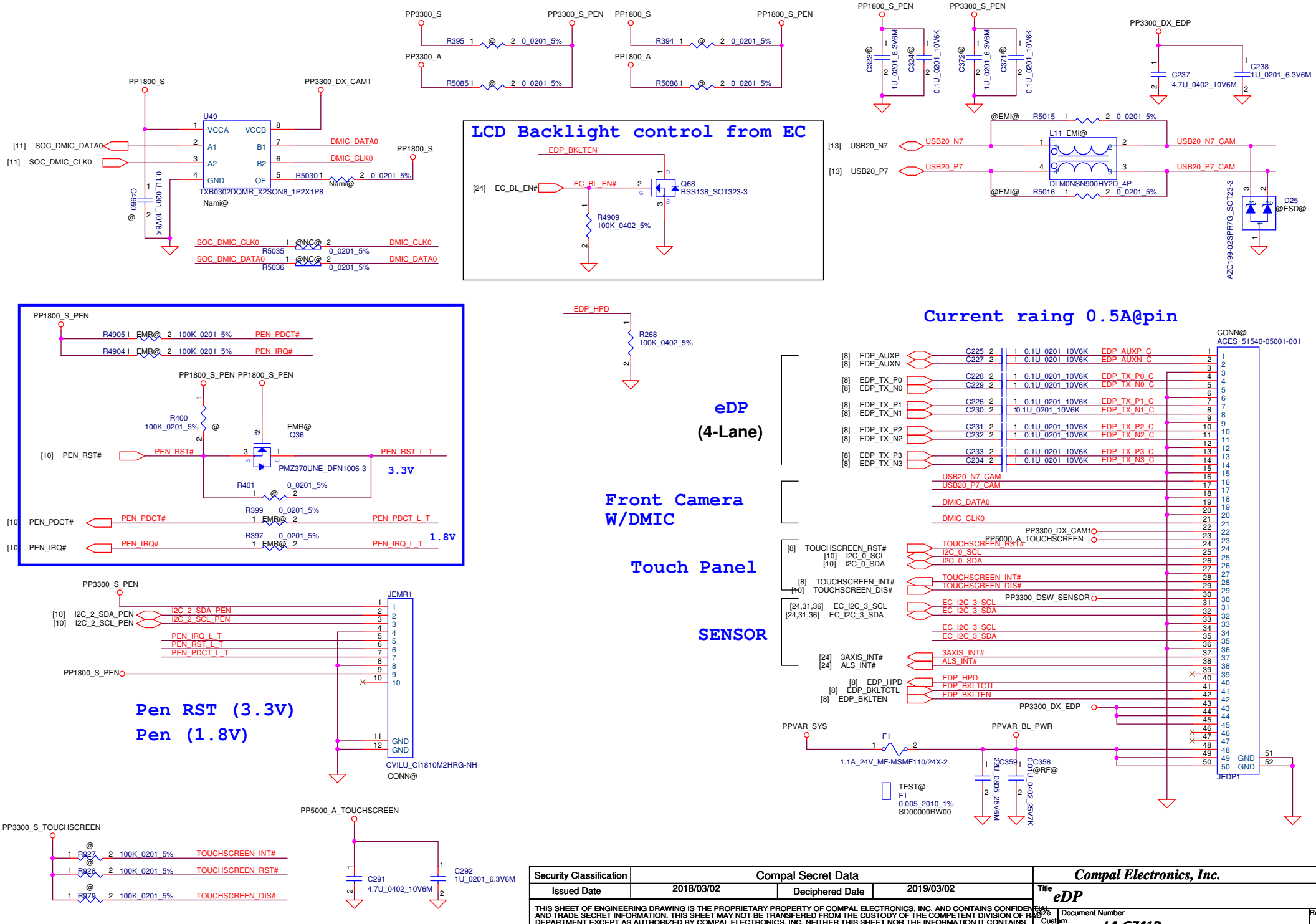

Security Classification	Compal Secret Data		
Issued Date	2018/03/02	Deciphered Date	2019/03/02

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Compal Electronics, Inc.

Title: eDP

Size: Custom | Document Number: LA-G741P | Rev: 1.0

Date: Thursday, July 19, 2018 | Sheet 28 of 54

KEY E

BLANK

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Issued Date	2018/03/02	Deciphered Date	2019/03/02

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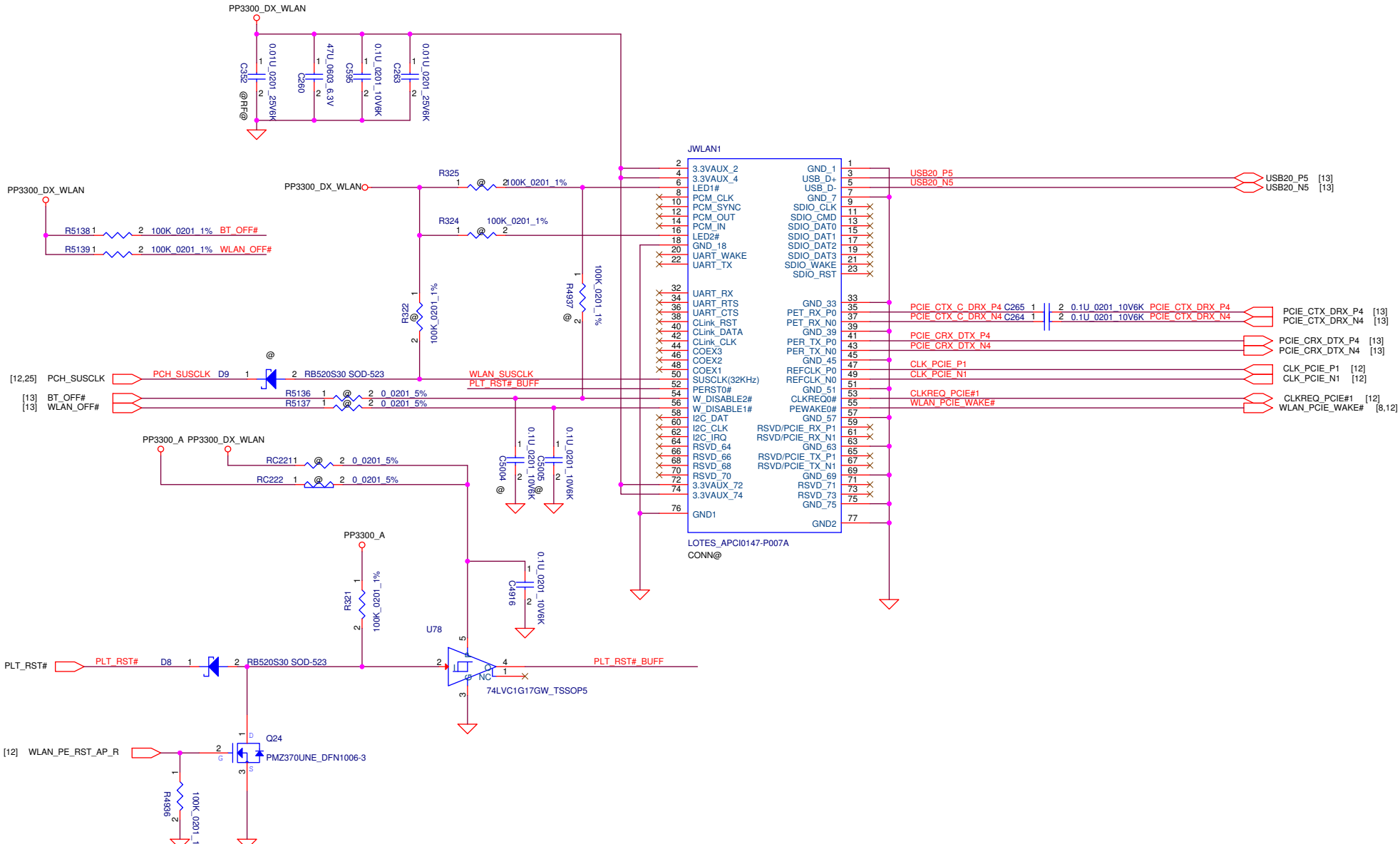
Compal Electronics, Inc.		
Title: Blank		
Size: Custom	Document Number: LA-G741P	Rev: 1.0
Date: Thursday, July 19, 2018	Sheet 29 of 54	

NGFF WiFi/BT (KEY E)



Security Classification	Compal Secret Data		
Issued Date	2018/03/02	Deciphered Date	2019/03/02

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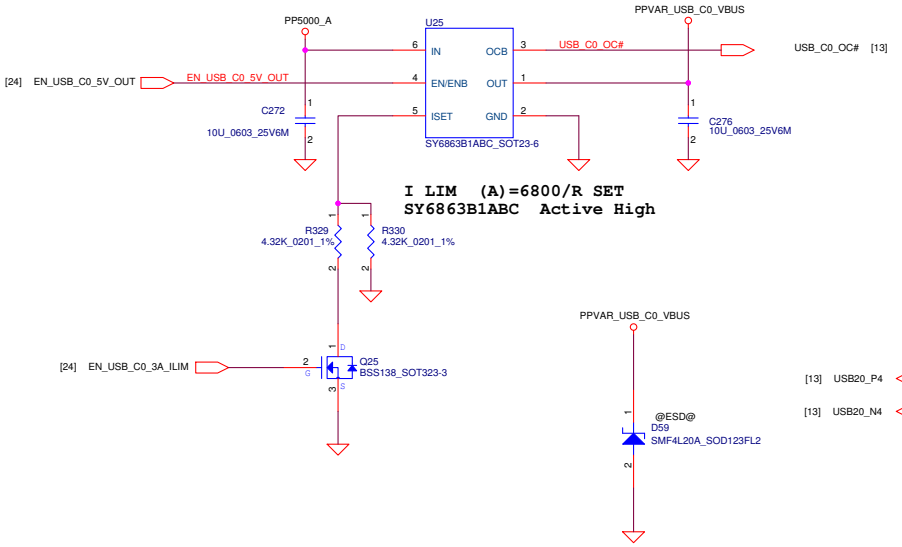
Compal Electronics, Inc.

Title: M.2 WLAN CONNECTOR

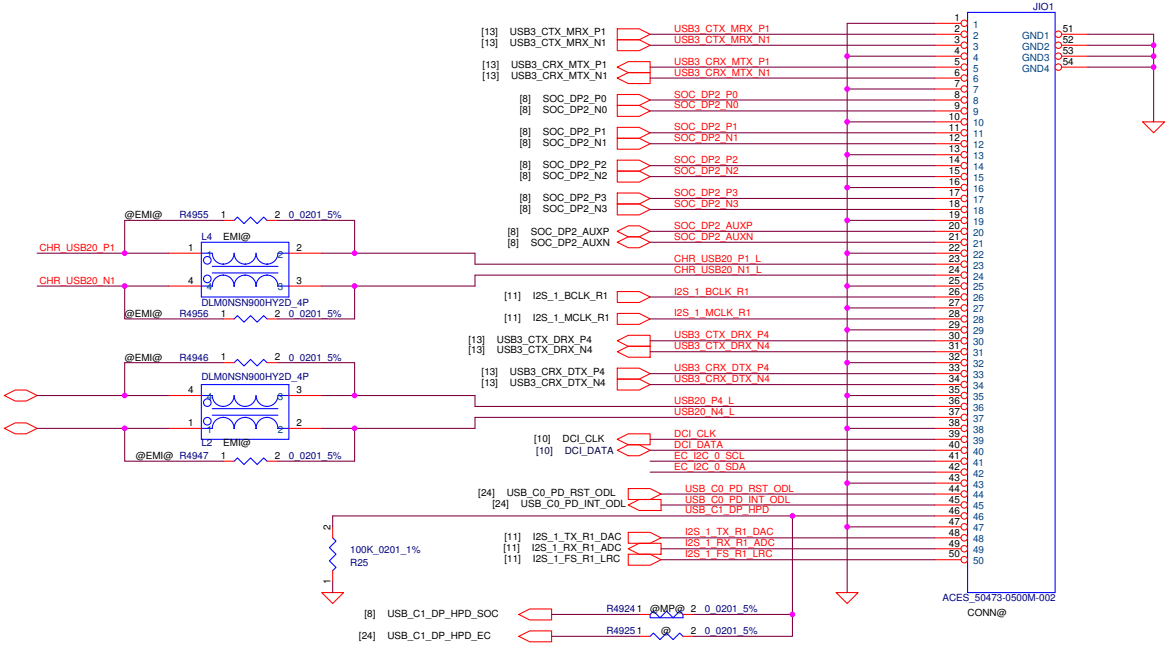
Size: Custom | Document Number: LA-G741P | Rev: 1.0

Date: Thursday, July 19, 2018 | Sheet 30 of 54

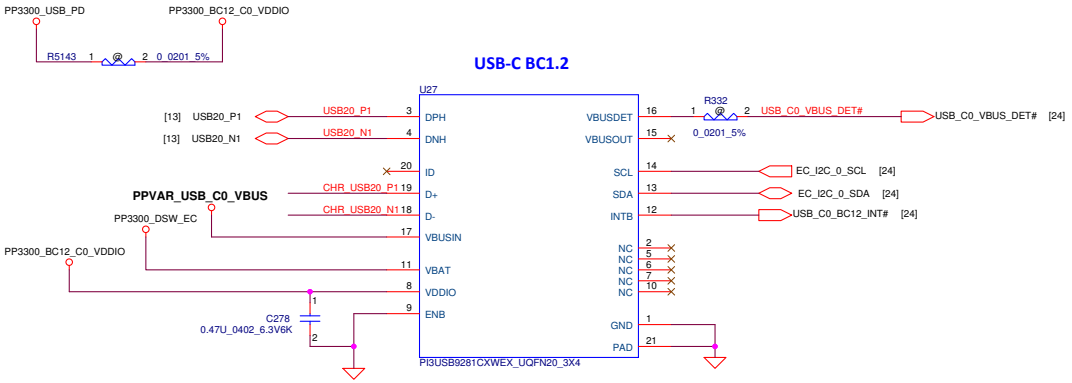
TYPE-C 5V POWER SWITCH

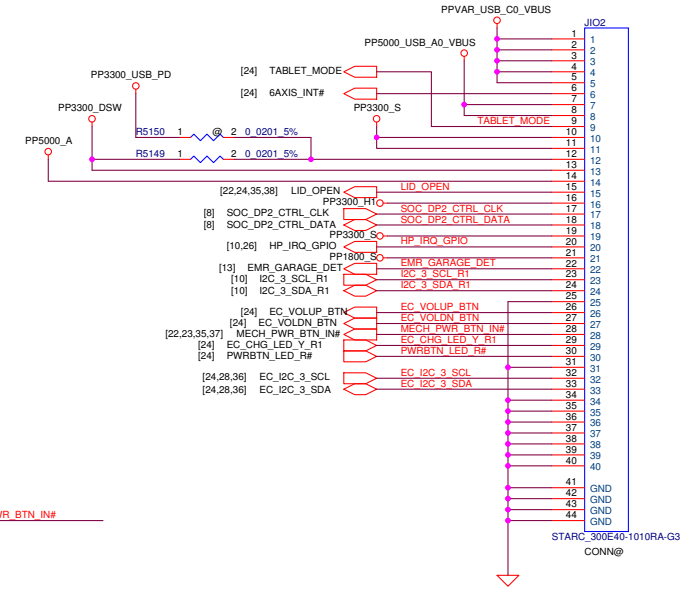


Sub Board 1 (LS-G222)



USB-C BC1.2





Security Classification	Compal Secret Data		
Issued Date	2018/03/02	Deciphered Date	2019/03/02

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Compal Electronics, Inc.

Title: USB TyecC DB

Size: A3 | Document Number: LA-G741P | Rev: 1.0

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The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP or EC's IO type is 1.8V, select 1.8V power for DVDD_IO.
If AP or EC's IO type is 3.3V, select 3.3V power for DVDD_IO.

PP3300_USB_PD
PP3300_USB_PD_ANX_AVDD
FB21 BLM03AG241SN1D_2P
C4967 1U_0402_16V6K
C4968 0.1U_0201_10V6K
C4969 100P_0201_25V7K
Closed Pin 13 and Pin 24.
PP3300_USB_PD_ANX_DVDD
C5008 @ 1U_0402_16V6K
R5067 @ 0_0402_5%
C4971 0.1U_0201_10V6K
Closed Pin 39.

U115
ANX3447QN-AC-R_QFN48_6X6

[8] SOC_DP1_P0	SOC_DP1_P0	R5117 @MP@ 0_0201_5%	SOC_DP1_P0_R	1	DP_LN_0P
[8] SOC_DP1_N0	SOC_DP1_N0	R5118 @MP@ 0_0201_5%	SOC_DP1_N0_R	2	DP_LN_0N
[8] SOC_DP1_P1	SOC_DP1_P1	R5119 @MP@ 0_0201_5%	SOC_DP1_P1_R	7	DP_LN_1P
[8] SOC_DP1_N1	SOC_DP1_N1	R5120 @MP@ 0_0201_5%	SOC_DP1_N1_R	8	DP_LN_1N
[8] SOC_DP1_P2	SOC_DP1_P2	R5121 @MP@ 0_0201_5%	SOC_DP1_P2_R	9	DP_LN_2P
[8] SOC_DP1_N2	SOC_DP1_N2	R5122 @MP@ 0_0201_5%	SOC_DP1_N2_R	10	DP_LN_2N
[8] SOC_DP1_P3	SOC_DP1_P3	R5123 @MP@ 0_0201_5%	SOC_DP1_P3_R	3	DP_LN_3P
[8] SOC_DP1_N3	SOC_DP1_N3	R5124 @MP@ 0_0201_5%	SOC_DP1_N3_R	4	DP_LN_3N
[8] SOC_DP1_AUXP	SOC_DP1_AUXP	C4982 0.1U_0201_10V6K	SOC_DP1_AUXP_C	16	AUXP
[8] SOC_DP1_AUXN	SOC_DP1_AUXN	C4981 0.1U_0201_10V6K	SOC_DP1_AUXN_C	17	AUXN
	USB_C0_DP_HPD	R5048 @MP@ 0_0201_5%	USB_C0_DP_HPD_R	36	HPD
[13] USB3_CTX_MRX_P2	USB3_CTX_MRX_P2	R5129 @MP@ 0_0201_5%	USB3_CTX_MRX_P2_R	12	SSTX_P
[13] USB3_CTX_MRX_N2	USB3_CTX_MRX_N2	R5130 @MP@ 0_0201_5%	USB3_CTX_MRX_N2_R	11	SSTX_N
[13] USB3_CRX_MTX_P2	USB3_CRX_MTX_P2	R5131 @MP@ 0_0201_5%	USB3_CRX_MTX_P2_R	6	SSRX_P
[13] USB3_CRX_MTX_N2	USB3_CRX_MTX_N2	R5132 @MP@ 0_0201_5%	USB3_CRX_MTX_N2_R	5	SSRX_N
[24] USB_C1_PD_RST_ODL	USB_C1_PD_RST_ODL	R5140 @MP@ 0_0201_5%	USB_C1_PD_RST_ODL_R	46	TEST_R
[24,33] EC_I2C0_1_SDA	EC_I2C0_1_SDA			37	CFG_SDA
[24,33] EC_I2C0_1_SCL	EC_I2C0_1_SCL			38	CFG_SCL
[24,33] EN_USB_C1_5V_OUT	R5083 @ 0_0201_5%	SINK_CTRL		43	SINK_CTRL
[24,42] EN_USB_C1_CHARGE_EC	R4984 @ 0_0201_5%	SOURCE_CTRL		44	SOURCE_CTRL
TP927 @	TEST_EN			45	TEST_EN
	VBUS_C1_DISCHG			35	DISCHARGE_CTRL
	ROLE_SELECT			28	ROLE_SELECT
	PD2_ADD0			48	I2C_ADR_0
	PD2_ADD1			47	I2C_ADR_1

				13	AVDD33
				24	AVDD33
				39	DVDD_IO
				25	SSTXP1
				26	SSTXN1
				33	SSRXN2
				34	SSRXP2
				30	SSTXP2
				29	SSTXN2
				32	SSRXN1
				31	SSRXP1
				19	SBU1
				18	SBU2
				22	CC1
				21	CC2
				23	VCONN_POWER
				41	FF0
				42	FF1
				40	INTP_OUT
				15	VBUS_SENSE
				20	VBUS_OCP
				14	NC
				27	NC
				49	VSS

USB3_DP1_1_MTX_DRX_P1	C4992 0.1U_0201_10V6K	USB3_DP1_1_MTX_C_DRX_P1	USB3_DP1_1_MTX_C_DRX_P1 [33]
USB3_DP1_1_MTX_DRX_N1	C4993 0.1U_0201_10V6K	USB3_DP1_1_MTX_C_DRX_N1	USB3_DP1_1_MTX_C_DRX_N1 [33]
USB3_DP1_2_MRX_DTX_N1			USB3_DP1_2_MRX_DTX_N1 [33]
USB3_DP1_2_MRX_DTX_P1			USB3_DP1_2_MRX_DTX_P1 [33]
USB3_DP1_2_MTX_DRX_P1	C4995 0.1U_0201_10V6K	USB3_DP1_2_MTX_C_DRX_P1	USB3_DP1_2_MTX_C_DRX_P1 [33]
USB3_DP1_2_MTX_DRX_N1	C4996 0.1U_0201_10V6K	USB3_DP1_2_MTX_C_DRX_N1	USB3_DP1_2_MTX_C_DRX_N1 [33]
USB3_DP1_1_MRX_DTX_N1			USB3_DP1_1_MRX_DTX_N1 [33]
USB3_DP1_1_MRX_DTX_P1			USB3_DP1_1_MRX_DTX_P1 [33]
DP1_AUXP_SBU1			
DP1_AUXN_SBU2			
USB_C1_CC1			USB_C1_CC1 [23,33]
USB_C1_CC2			USB_C1_CC2 [23,33]

PP5000_A
R5049 1M_0201_5%
R5050 1M_0201_5%
C4965 EMI@ 1000P_0201_25V7K
C4966 EMI@ 1000P_0201_25V7K
C4991 4.7U_0402_6.3V6M

VCONN_POWER is the power source for VCONN:
1) VCONN Voltage range [3.6V, 5.5V]
2) Internal VCONN Switch:Iout Max 400mA,Rdson Max 1.2 ohm
2) VCONN Minimum power is 1W. If DP Alternate
Mode is supported, VCONN power is up to 1.5W.

USB_C1_PD_INT_ODL [24]
PPVAR_USB_C1_VBUS_L
R4983 2 348K_0201_1%
TP945 @
R5065 49.9K_0201_1%

PP3300_USB_PD
R5068 2 100K_0201_1% SOC_DP1_AUXN_C
R5069 2 100K_0201_1% SOC_DP1_AUXP_C

PP3300_USB_PD_ANX_DVDD
R5051 2 1.8K_0201_1% EC_I2C0_1_SDA
R5052 2 1.8K_0201_1% EC_I2C0_1_SCL

PPVAR_USB_C1_VBUS_L
R5053 1.2K_0402_5%
Q77 PMZ370UNE_DFN1006-3
R5054 100K_0201_5% @
DISCHARGE_CTRL
Auto VBUS discharge pin.
Internal 100K pull down.

PP3300_USB_PD_ANX_AVDD
R5055 2 4.7K_0201_5% ROLE_SELECT
R5058 @ 2 4.7K_0201_5%
ROLE_SELECT pin:
Logic 1: DRP Mode.
Logic 0: DFP Mode.
NC: UFP Mode.

[24] USB_C0_DP_HPD_EC R4927 @ 2 0_0201_5% USB_C0_DP_HPD
[8] USB_C0_DP_HPD_SOC R4926 1 @MP@ 2 0_0201_5%
R28 100K_0201_1%

PP5000_A
D42 RB751S-40 CCD@
R5110 CCD@ 100K_0201_1%
[23,24] CCD_MODE_ODL CCD_MODE_ODL
PP3300_H1
Q81 CCD@ PMZ370UNE_DFN1006-3

R5155 @ 2 0_0201_1%
Q79 CCD@ PMZ370UNE_DFN1006-3
DP1_AUXP_SBU1 USB_C1_SBU1 USB_C1_SBU1 [23,33]
C4994 EMI@ 1000P_0201_25V7K
R5070 2M_0201_5%
Q80 CCD@ PMZ370UNE_DFN1006-3
DP1_AUXN_SBU2 USB_C1_SBU2 USB_C1_SBU2 [23,33]
R5156 @ 2 0_0201_1%
C4997 EMI@ 1000P_0201_25V7K
R5071 2M_0201_5%
Closed U115
Closed U11
To H1

PP3300_USB_PD_ANX_DVDD
R5056 2 4.7K_0201_5% PD2_ADD0
R5059 2 4.7K_0201_5% PD2_ADD1
R5057 @ 2 4.7K_0201_5%
R5060 @ 2 4.7K_0201_5%

I2C_ADR_1/I2C_ADR_0:
Input pin with internal 100k ohm pull-down

I2C_ADR_1	I2C_ADR_0	TCPC Address (Wakeup address)	SPI Address	EMTB Address	EMTB Address	Debug Address_1	Debug Address_2
0	0	0x58	0x7E	0x7A	0x84	0x72	0x70
0	1	0x56	0x6E	0x78	0x86	0x76	0x70
1	0	0x54	0x64	0x68	0x6C	0x5C	0x70
1	1	0x52	0x62	0x6A	0x74	0x82	0x70

	Stuff	Unstuff
CCD mode:	Q79, Q80, Q81, D42 and R5110	R5155 and R5156
Non CCD mode:	R5155 and R5156	Q79, Q80, Q81, D42 and R5110

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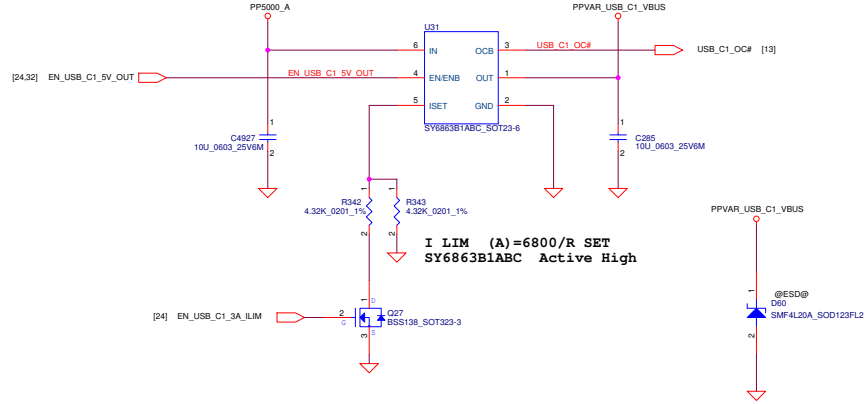
Compal Electronics, Inc.

Title: USB TyecC LOAD SWITCH

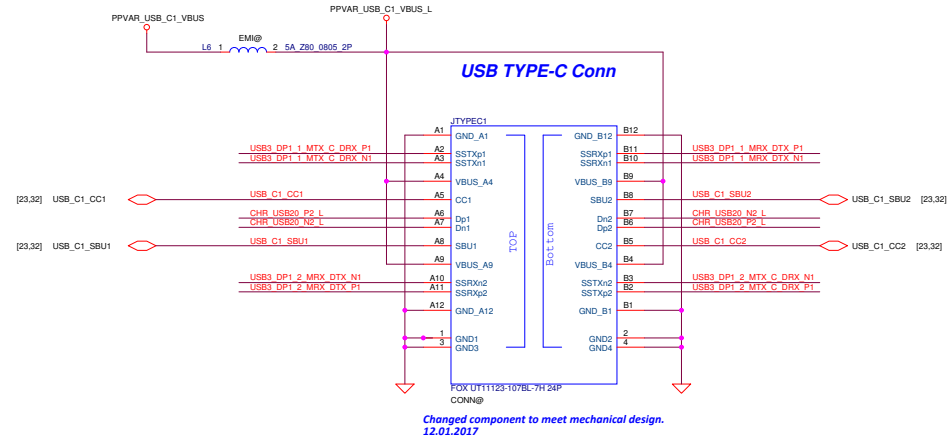
Size: A3 | Document Number: LA-G741P | Rev: 1.0

Date: Thursday, July 19, 2018 | Sheet 32 of 54

5V Current limit

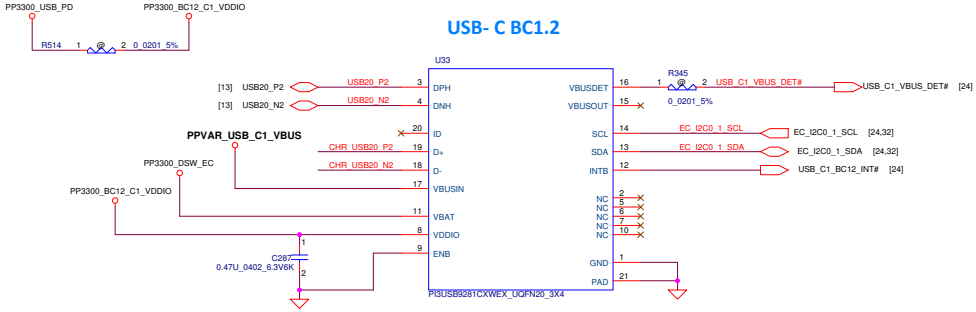


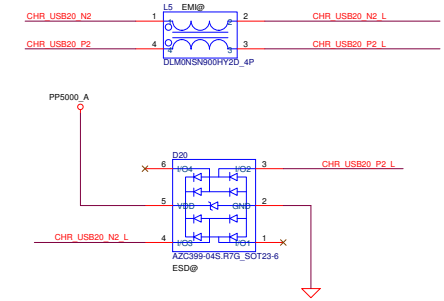
USB TYPE-C Conn

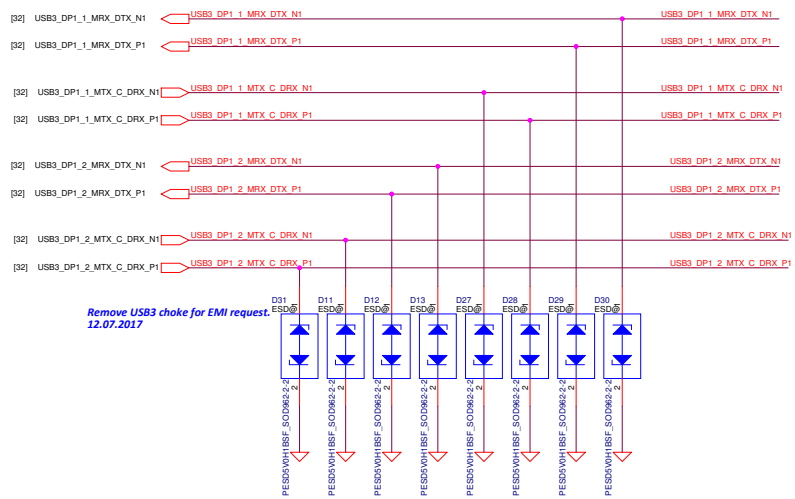


Changed component to meet mechanical design.
12.01.2017

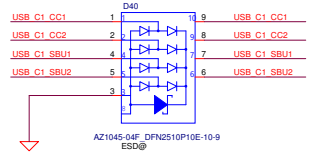
USB- C BC1.2

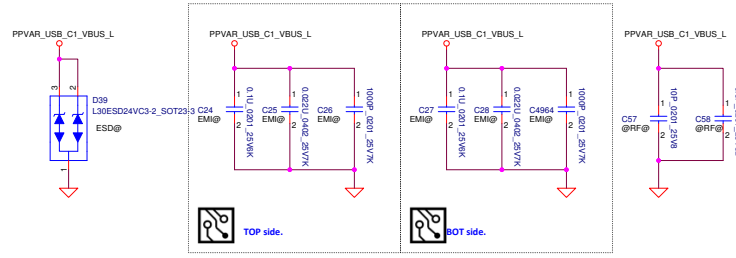






Remove USB3 choke for EMI request.
12.07.2017





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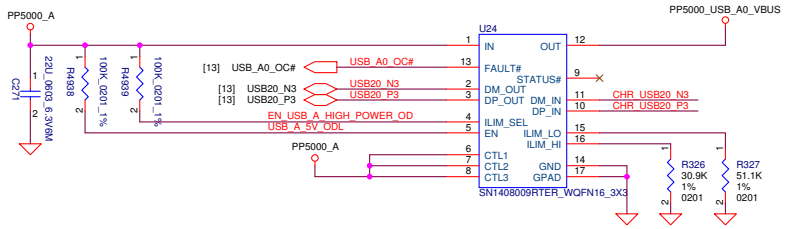
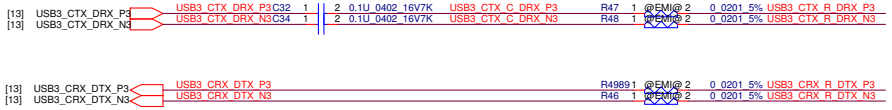
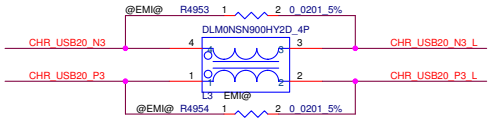
Compal Electronics, Inc.			
Title	USB3.0 Type-C Conn.		
Size	Document Number	LA-G741P	Rev 1.0
Custom	Date: Thursday, July 19, 2018	Sheet 33 of 54	

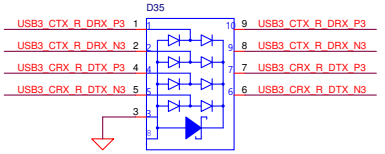
Type A BC1.2

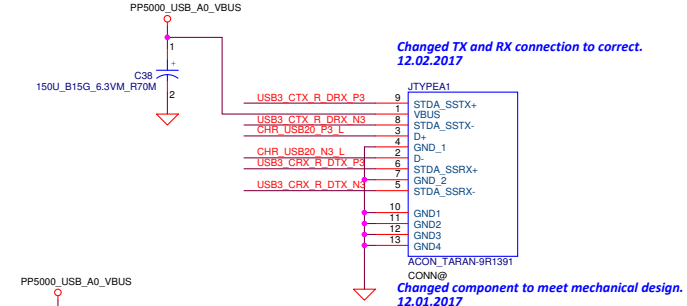


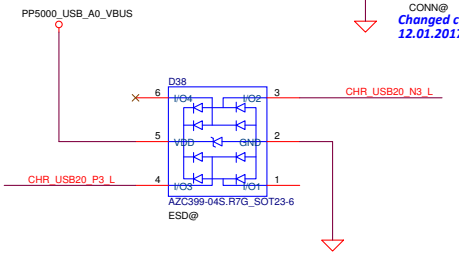
Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH (Discharge)	0	0	0	X
CDP	1	1	1	1
SDP2 (No Discharge from/to CDP)	1	1	1	0
SDP1 (Discharge from/to any charging state including CDP)	1	1	0	X
	0	1	0	X
DCP_SHORTED	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	1	1	X
	0	0	1	X



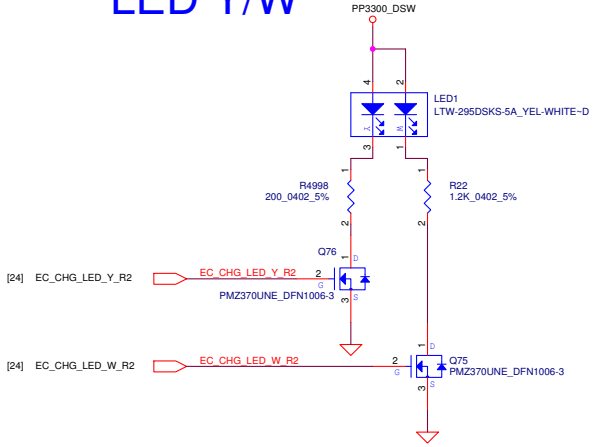








LED Y/W



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Issued Date	2018/03/02	Deciphered Date	2019/03/02

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Compal Electronics, Inc.			
Title	USB Type-A / LED		
Size: Custom	Document Number: LA-G741P		Rev: 1.0
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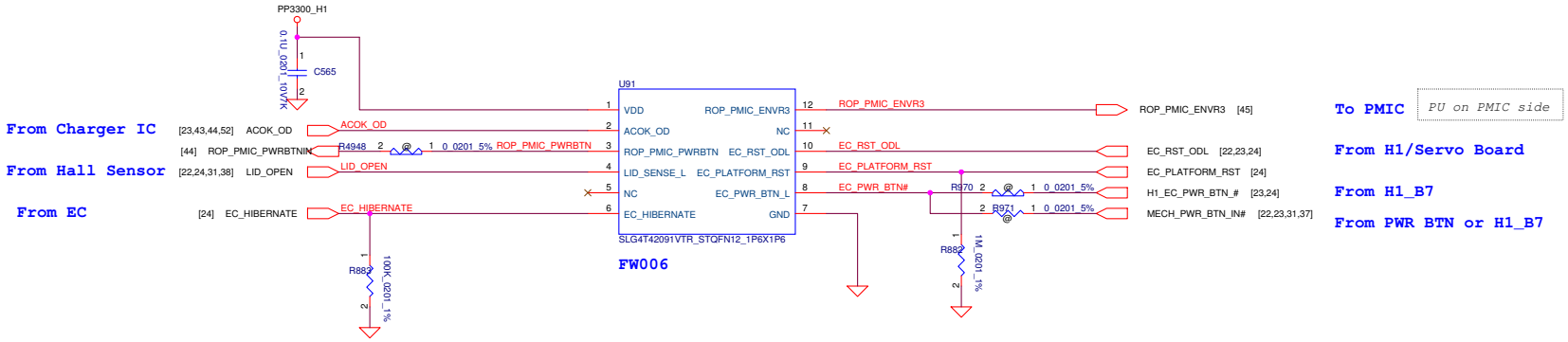

Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	ACOK_OD	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	ROP_PMIC_PWRBTN	Digital Output	Open Drain NMOS 1X	floating
4	LID_SENSE_L	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
5	NC	--	Keep Floating or Connect to GND	--
6	EC_HIBERNATE	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
7	GND	GND	Ground	--
8	EC_PWR_BTN_L	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
9	EC_PLATFORM_RST	Digital Input	Digital Input with Schmitt trigger	1MΩ pulldown
10	EC_RST_ODL	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	100kΩ pullup
11	NC	--	Keep Floating or Connect to GND	--
12	ROP_PMIC_ENVR3	Digital Output	Open Drain NMOS 1X	floating

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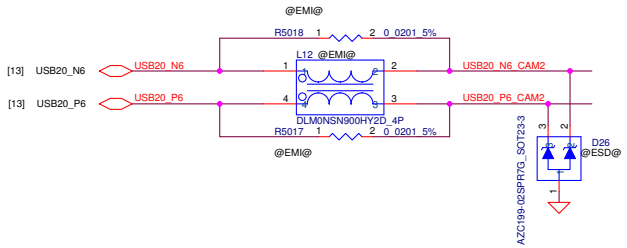
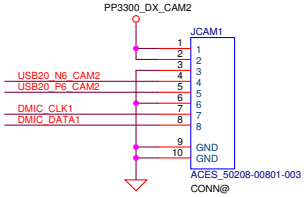
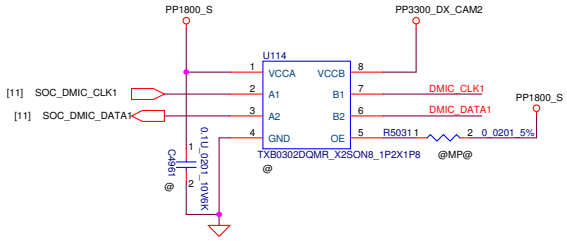
Compal Electronics, Inc.	
Title	HIBERNATE WAKE SOURCE
Size: Custom	Document Number: LA-G741P
Rev	1.0
Date: Thursday, July 19, 2018	Sheet 35 of 54

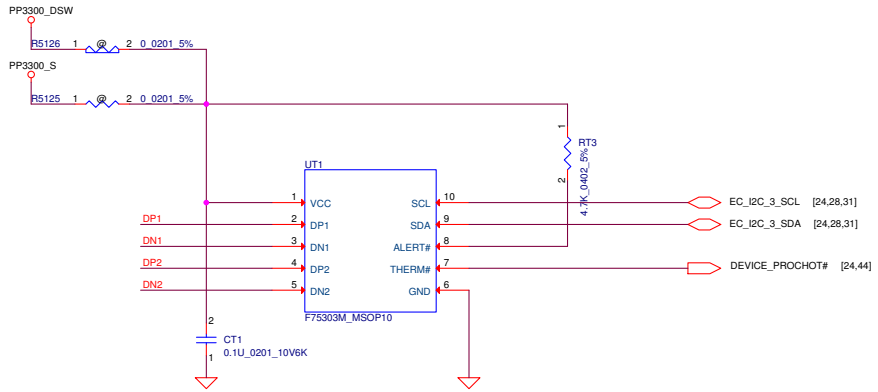


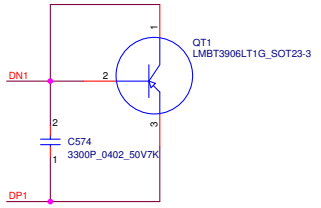
Rear Camera W/ DMIC

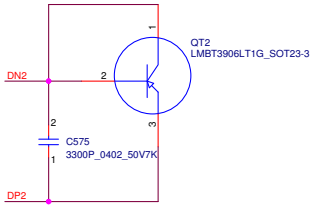




Thermal Sensor

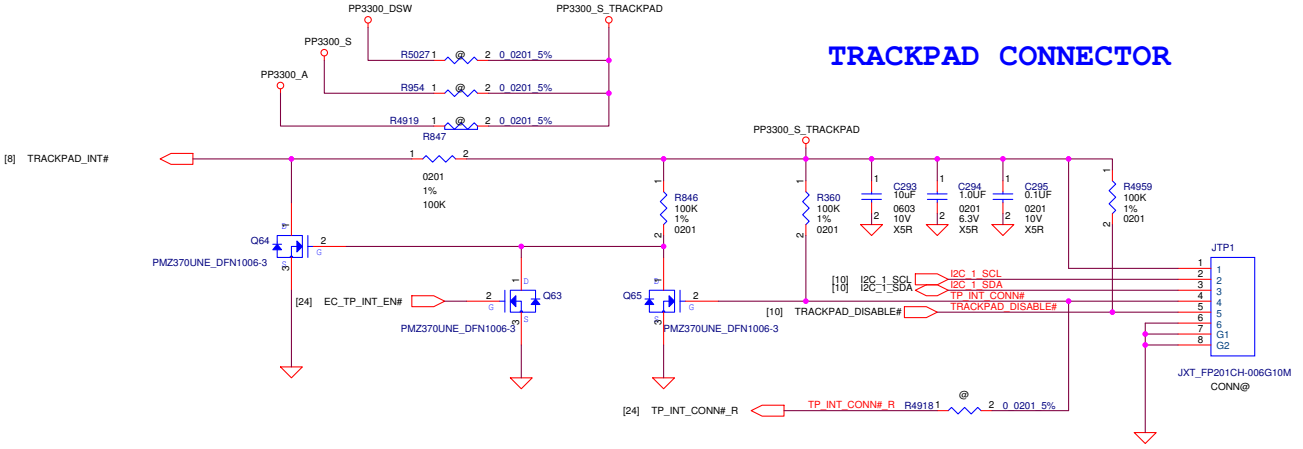






Close SOC

Close POWER IC



TRACKPAD CONNECTOR

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Issued Date	2018/03/02	Deciphered Date	2019/03/02

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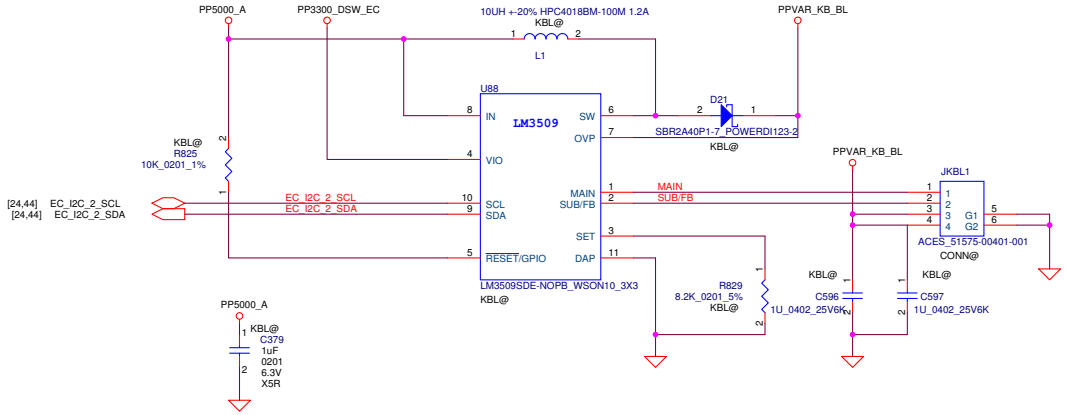
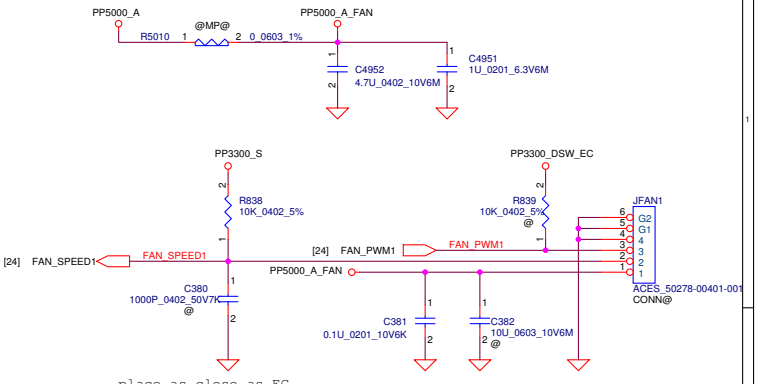
Compal Electronics, Inc.			
Title: Touch, Trapckpad, Pen			
Size:	Document Number: LA-G741P		Rev: 1.0
Date: Thursday, July 19, 2018	Sheet 36 of 54		

KEYBOARD BACKLIGHT



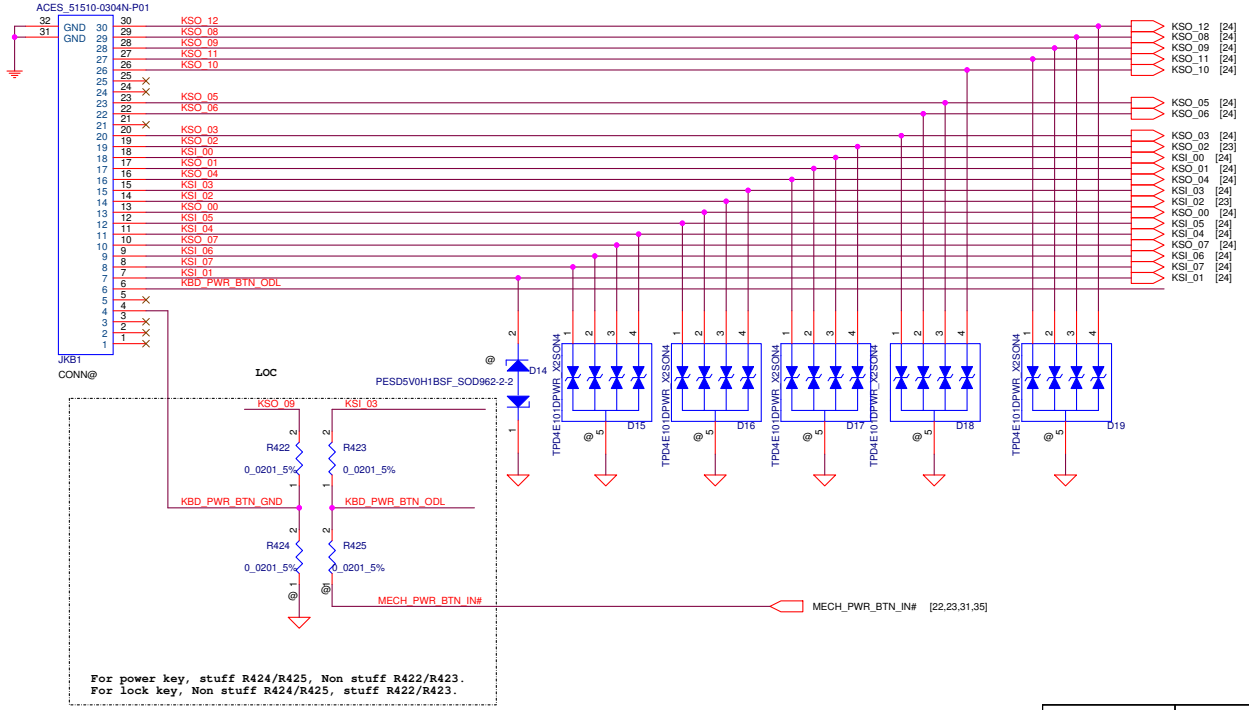
ILED_MAX = 192×1.244V/RSET.
==>192 X 1.244/2.2K = 108 mA

CPU Fan Control Circuit



ODM TO CHOOSE CONNECTOR

KEYBOARD



For power key, stuff R424/R425, Non stuff R422/R423.
For lock key, Non stuff R424/R425, stuff R422/R423.

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Compal Electronics, Inc.			
Title: KB, KB Backlight, FAN			
Size: Custom	Document Number: LA-G741P		Rev: 1.0
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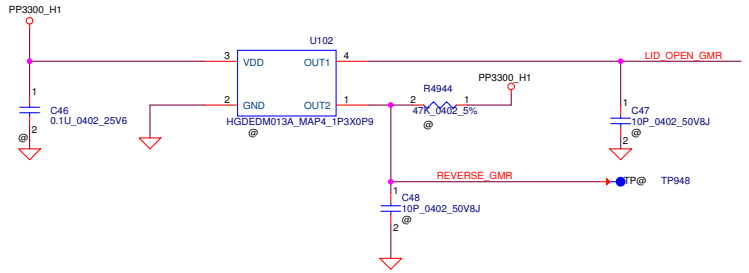

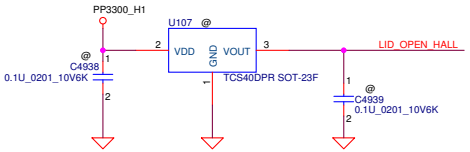

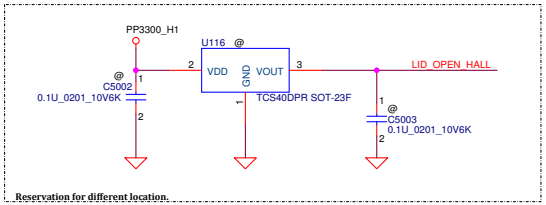

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Title: **LID Sensor**

Size	Document Number	Rev
Custom	LA-G741P	1.0

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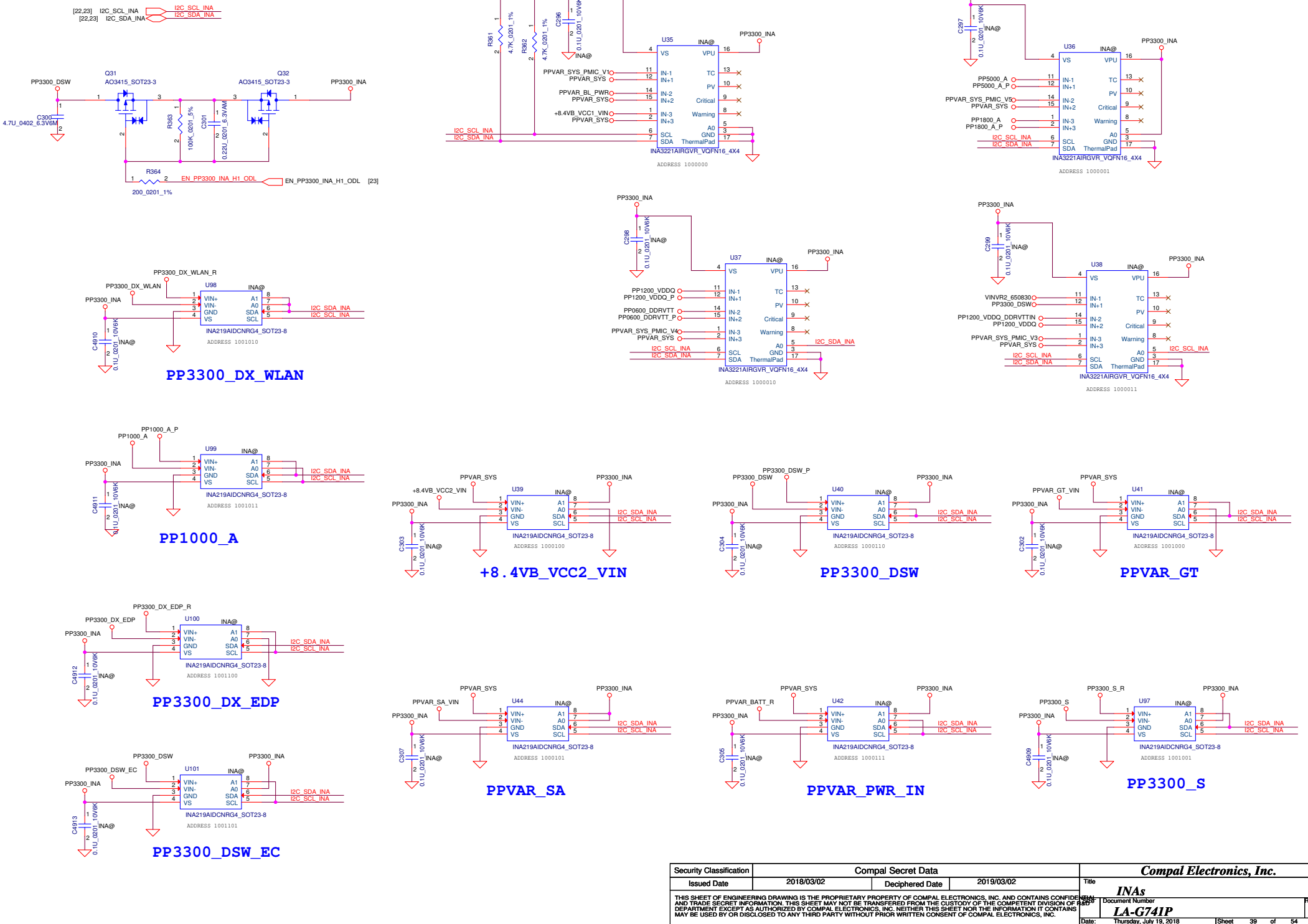

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Issued Date	2018/03/02	Deciphered Date	2019/03/02

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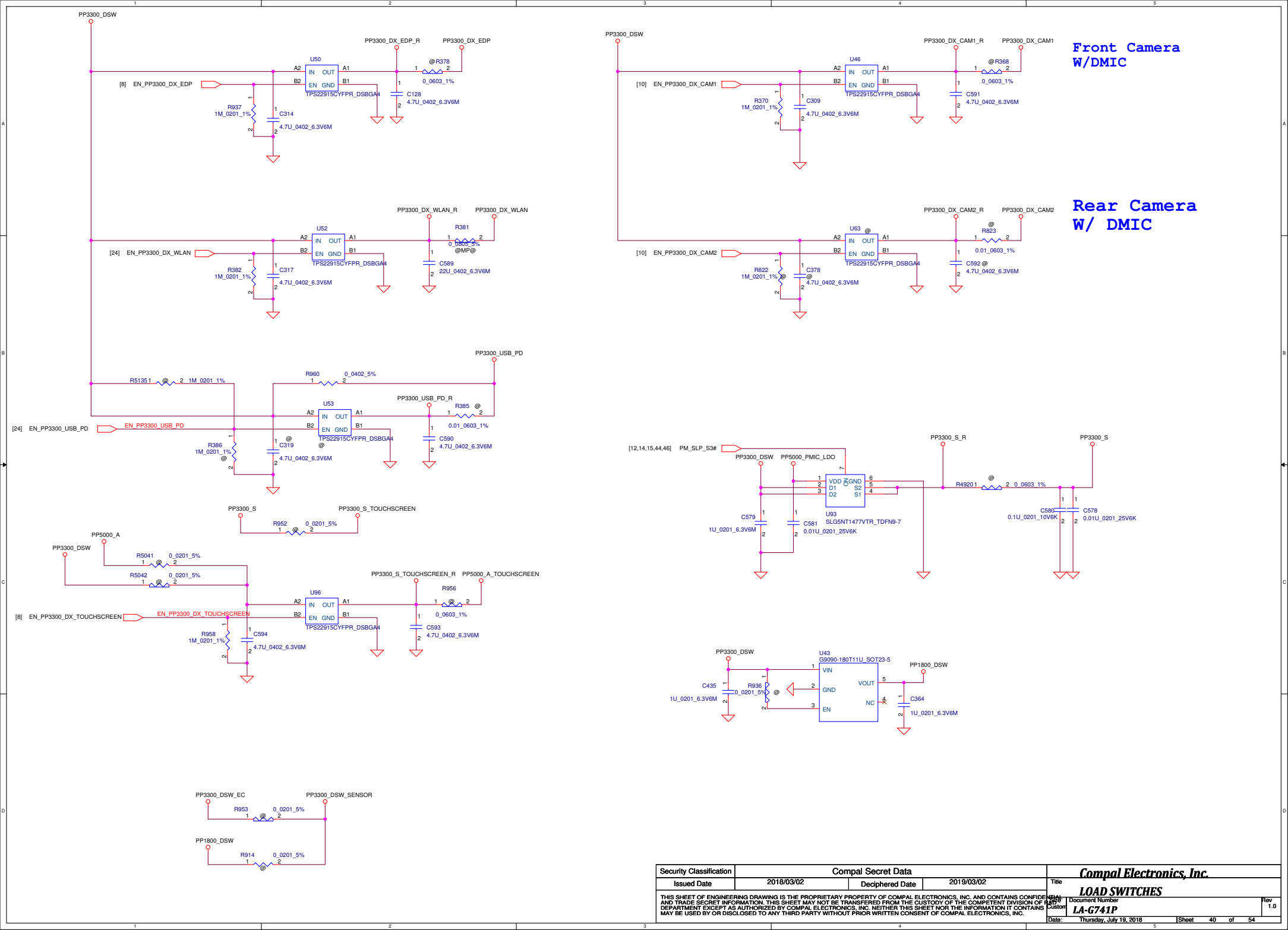
Compal Electronics, Inc.	
Title	INAs
Size	Document Number: LA-G741P
Rev	1.0
Date:	Thursday, July 19, 2018
Sheet	39 of 54



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Issued Date	2018/03/02	Deciphered Date	2019/03/02

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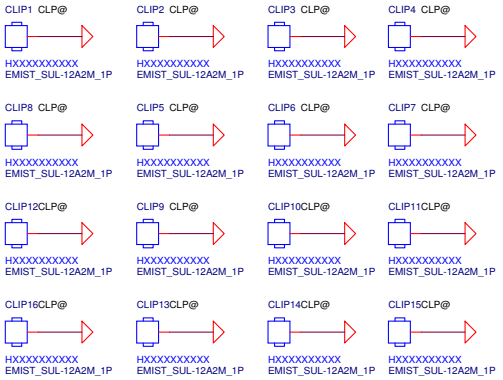
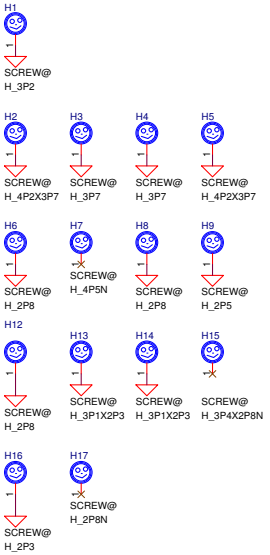
Compal Electronics, Inc.			
Title: LOAD SWITCHES			
Size: Custom	Document Number: LA-G741P		Rev: 1.0
Date: Thursday, July 19, 2018	Sheet 40 of 54		

[CLIP]



[Screw Hole]



Security Classification	Compal Secret Data		
Issued Date	2018/03/02	Deciphered Date	2019/03/02

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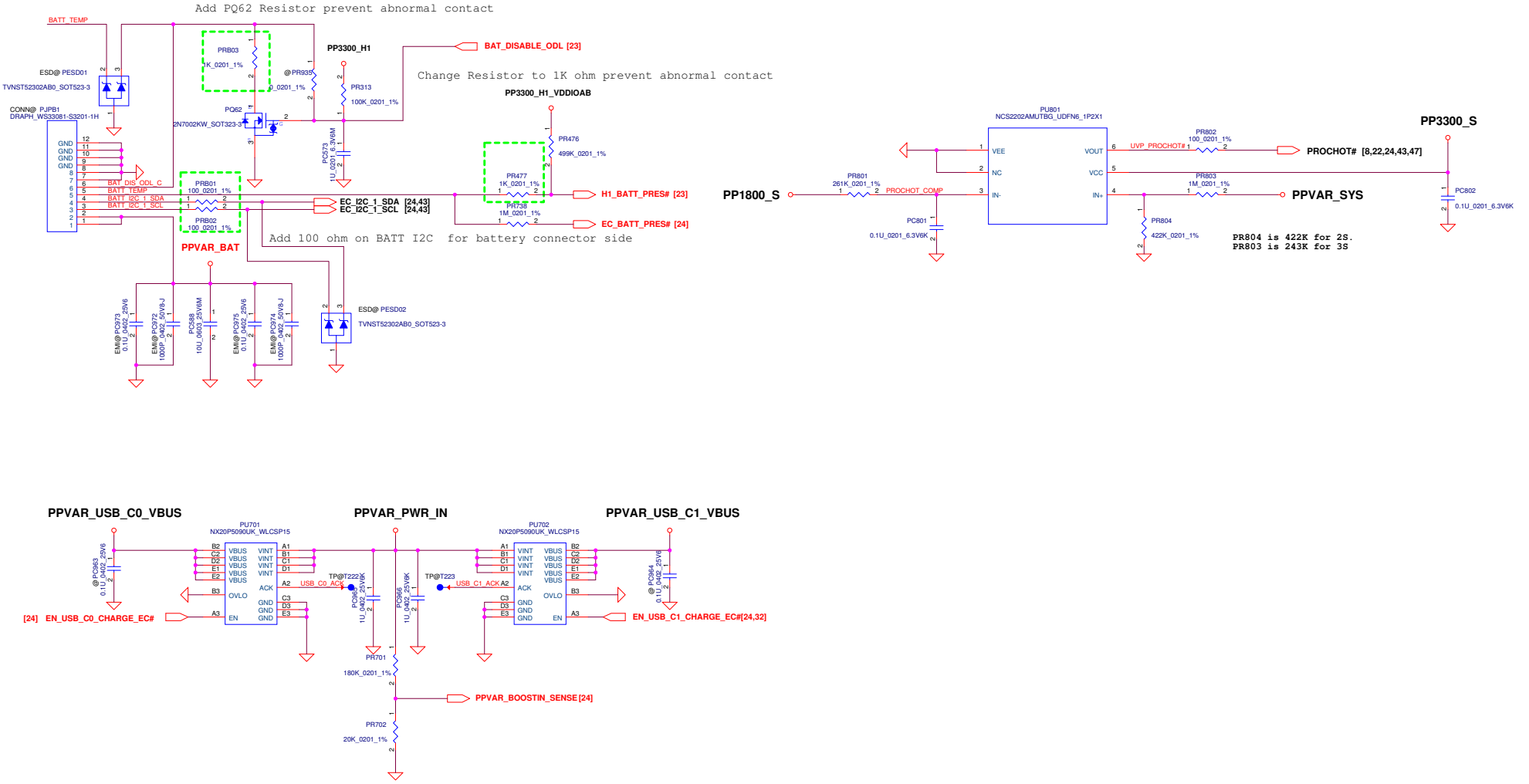
Compal Electronics, Inc.			
Title: PCB, Screw, CLIP			
Size: Custom	Document Number: LA-G741P		Rev: 1.0
Date: Thursday, July 19, 2018	Sheet 41 of 54		



Security Classification	Compal Secret Data		
Issued Date	2017/06/20	Deciphered Date	2018/06/20

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Title			
Size: Custom	Document Number		Rev 0.1
Date: Thursday, July 19, 2018	Sheet 42 of 54		

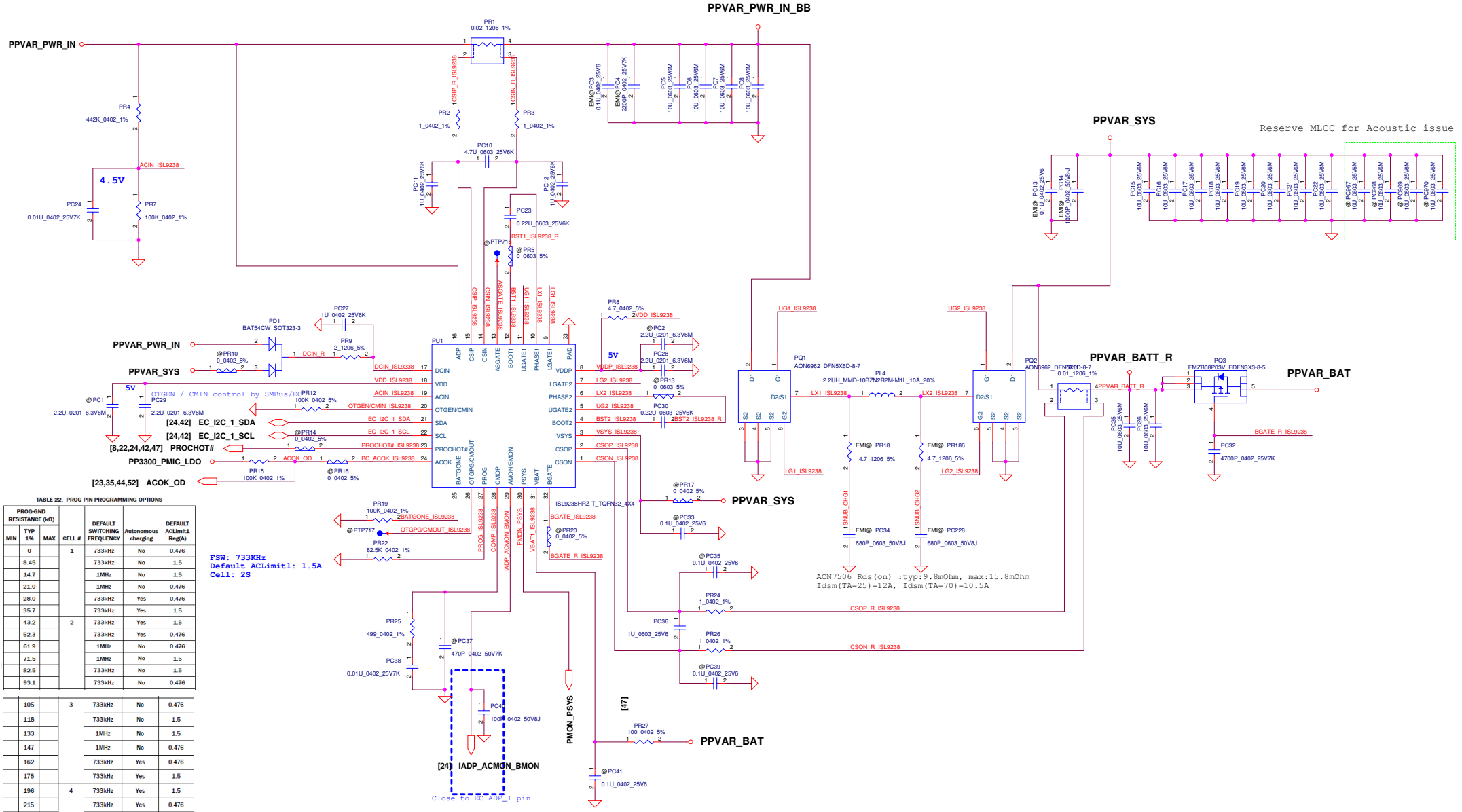

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)			CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
MIN	TYP 1%	MAX				
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: CHARGER ISL9238			
Size: Custom	Document Number		Rev: 0.1
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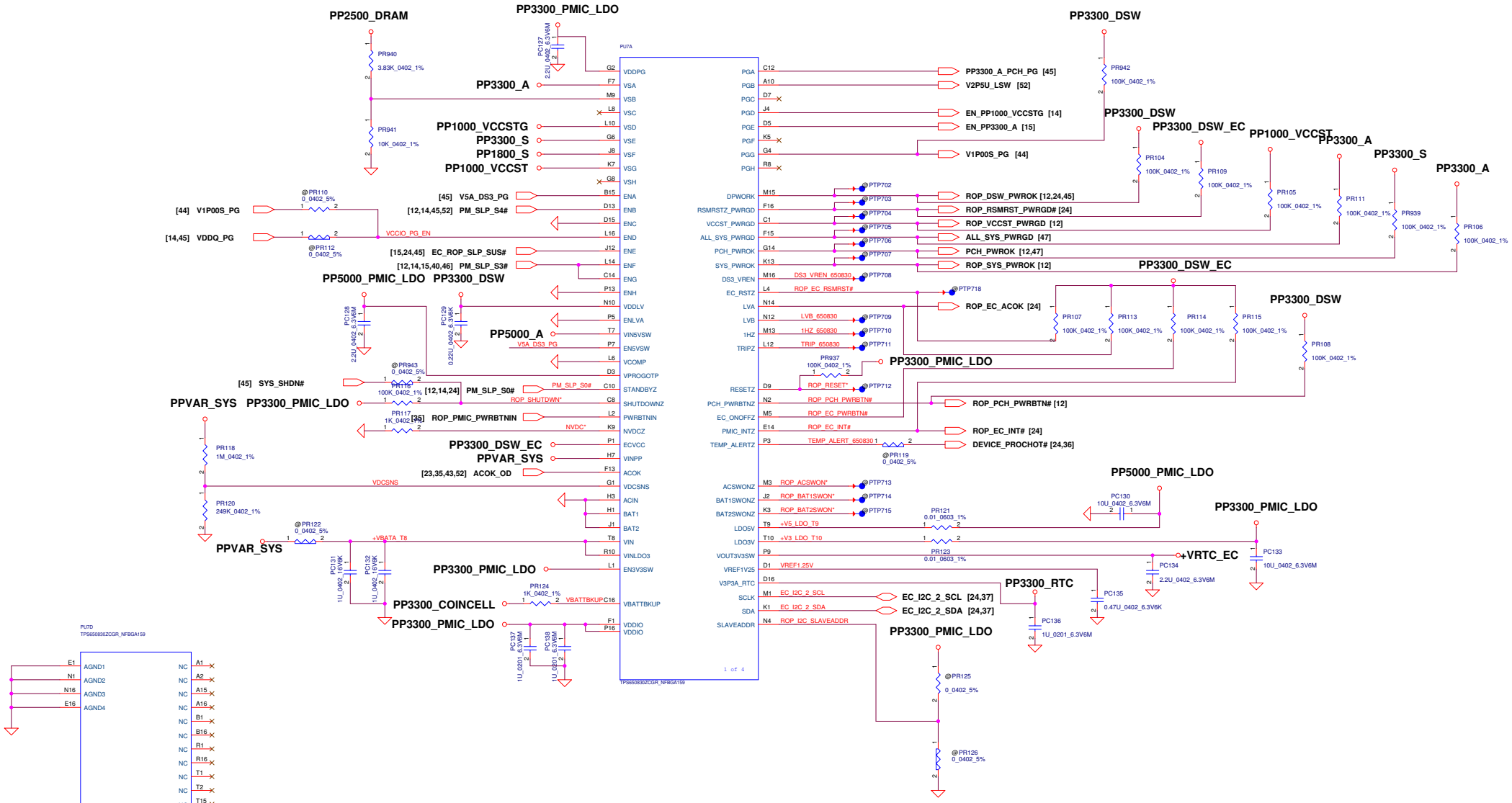

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PWR_PMIC-TPS650830(1of2)

Size: Custom | Document Number | Rev 0.1

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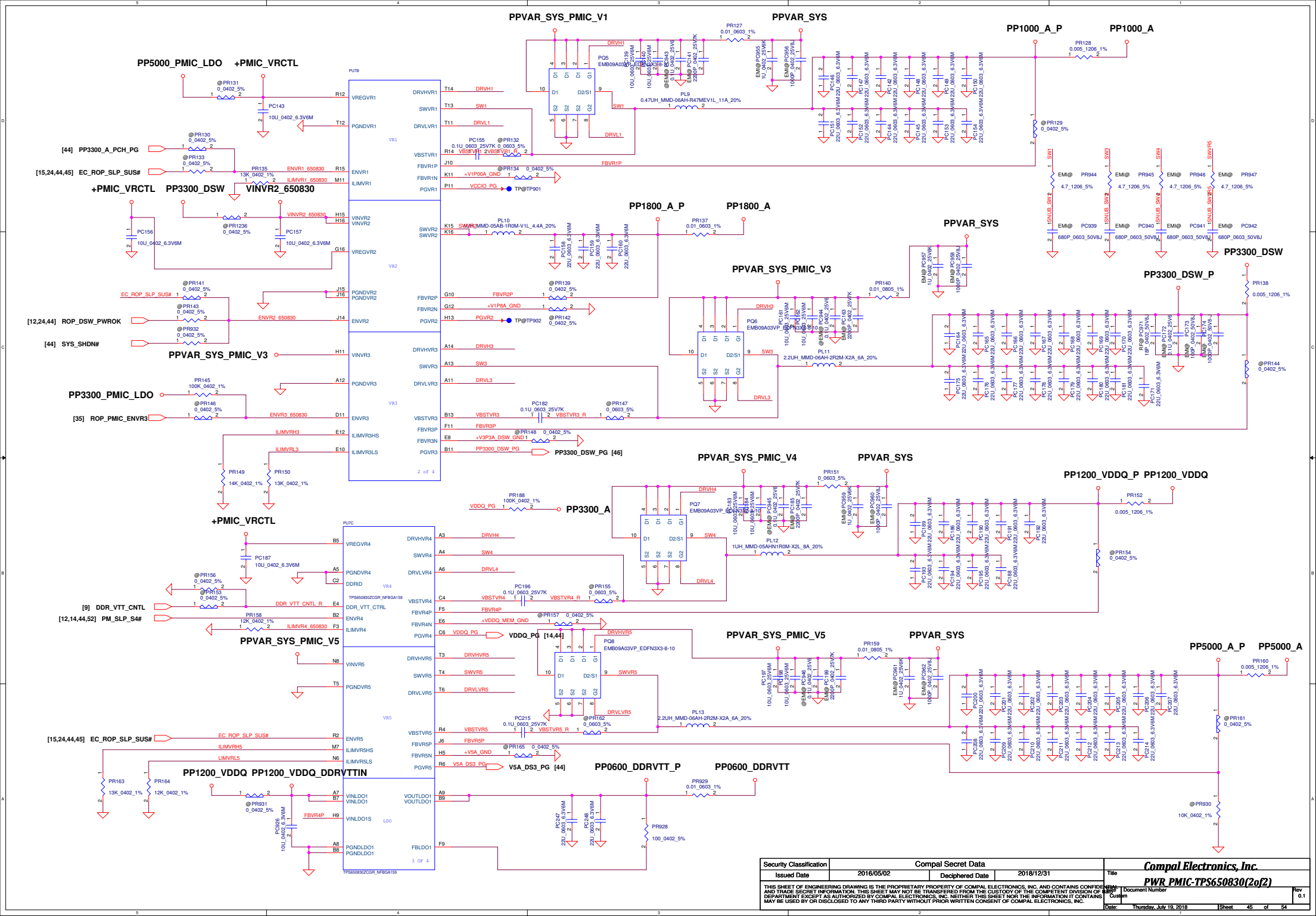
PPVAR_SYS_PMIC_V1
PPVAR_SYS
PP1000_A_P
PP1000_A
PP5000_PMIC_LDO
+PMIC_VRCTL
PU7B
VR1
VR2
VR3
2 of 4
[44] PP3300_A_PCH_PG
[15,24,44,45] EC_ROP_SLP_SUS#
+PMIC_VRCTL
PP3300_DSW
VINVR2_650830
PP1800_A_P
PP1800_A
PPVAR_SYS
PP3300_DSW
PPVAR_SYS_PMIC_V3
PP3300_DSW_P
[12,24,44] ROP_DSW_PWROK
[44] SYS_SHDN#
PP3300_PMIC_LDO
[35] ROP_PMIC_ENVR3
PP3300_DSW_PG [46]
PPVAR_SYS_PMIC_V4
PPVAR_SYS
PP1200_VDDQ_P
PP1200_VDDQ
PP3300_A
+PMIC_VRCTL
PU7C
VR4
VR5
3 OF 4
TPS650830ZCGR_NFBGA159
[9] DDR_VTT_CNTL
[12,14,44,52] PM_SLP_S4#
VDDQ_PG [14,44]
PPVAR_SYS_PMIC_V5
PPVAR_SYS
PP5000_A_P
PP5000_A
[15,24,44,45] EC_ROP_SLP_SUS#
PP1200_VDDQ
PP1200_VDDQ_DDRVTTIN
LDO
V5A_DS3_PG [44]
PP0600_DDRVTT_P
PP0600_DDRVTT
Security Classification
Compal Secret Data
Issued Date
2016/05/02
Deciphered Date
2018/12/31
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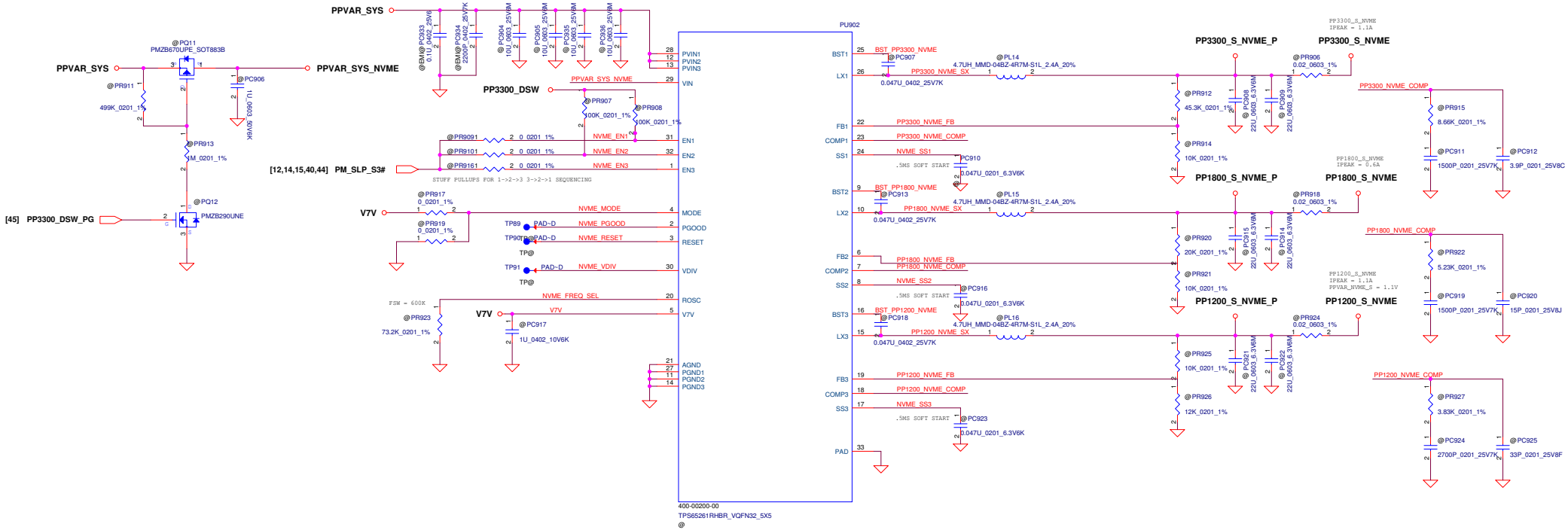
Compal Electronics, Inc.
Title
PWR_PMIC-TPS650830(2of2)
Size
Custom
Document Number
Rev
0.1
Date:
Thursday, July 19, 2018
Sheet
45
of
54



Security Classification	Compal Secret Data		
Issued Date	2016/05/02	Deciphered Date	2018/12/31

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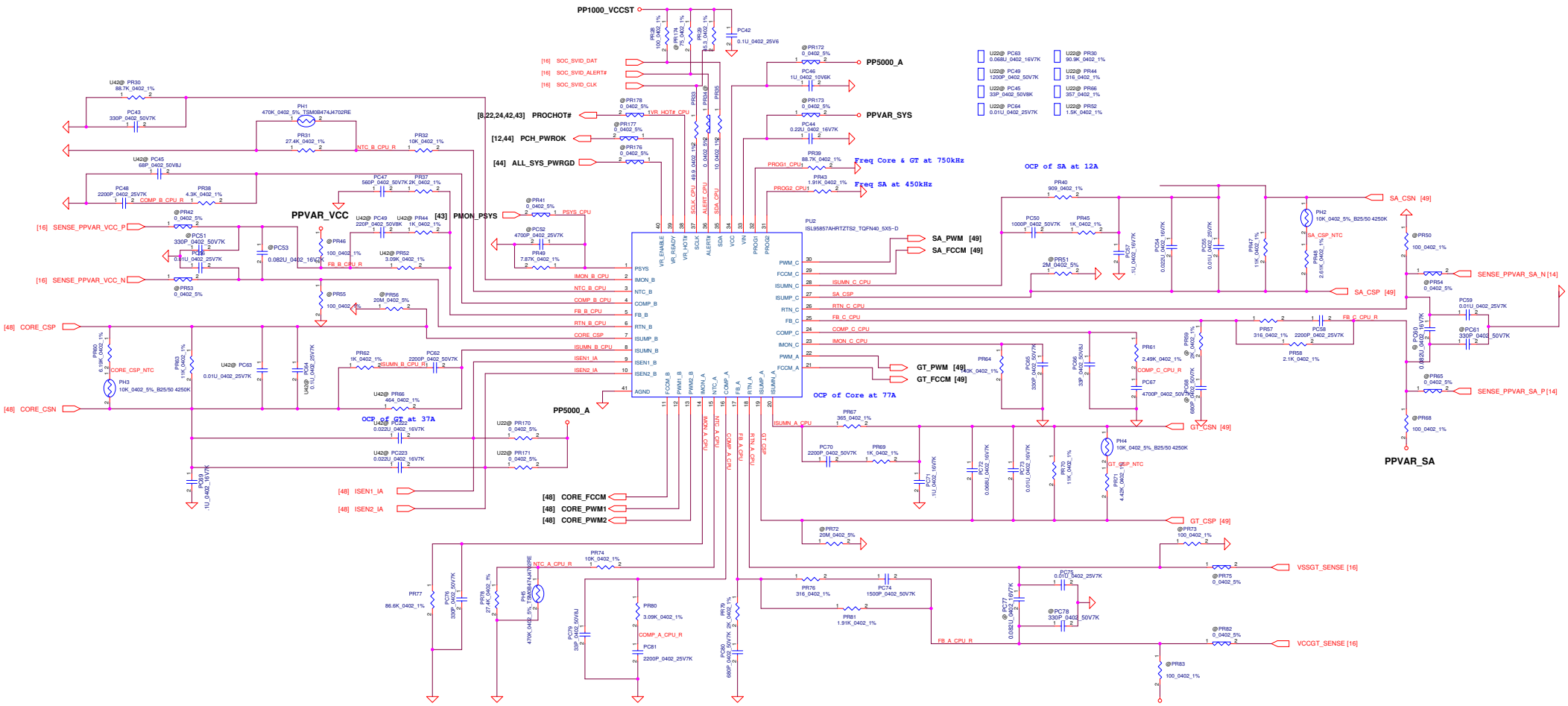
Compal Electronics, Inc.

Title: PWR_NVMe

Size: Custom | Document Number | Rev 0.1

Date: Thursday, July 19, 2018 | Sheet 46 of 54



Security Classification	Compal Secret Data		
Issued Date	2016/05/02	Deciphered Date	2018/12/31

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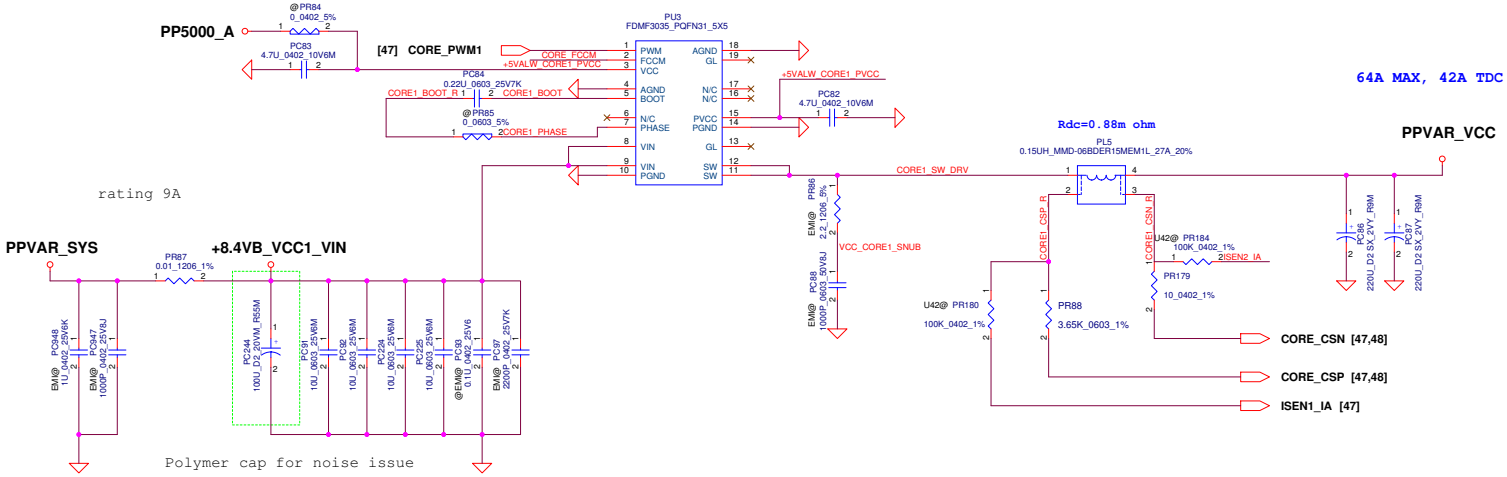
Compal Electronics, Inc.

Title: PWR IMVP8(1of3)

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, July 19, 2018 | Sheet 47 of 54



Security Classification	Compal Secret Data		
Issued Date	2016/05/02	Deciphered Date	2018/12/31

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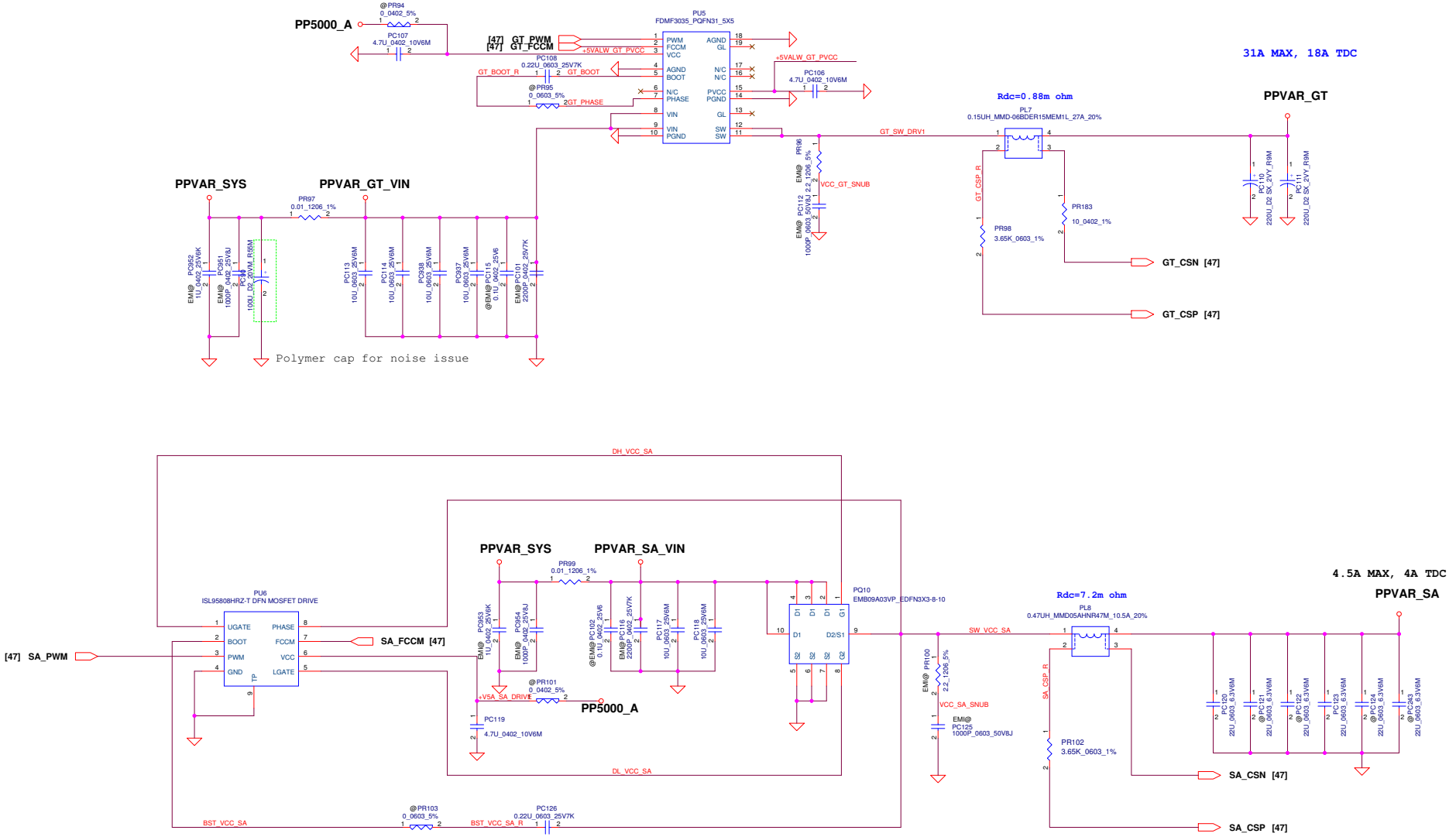
Compal Electronics, Inc.			
Title: PWR_IMVP8(2of3)			
Size: Custom	Document Number		Rev: 0.1
Date: Thursday, July 19, 2018	Sheet 48 of 54		



Security Classification	Compal Secret Data		
Issued Date	2016/05/02	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title: PWR IMVP8(3of3)

Size: Custom | Document Number | Rev 0.1

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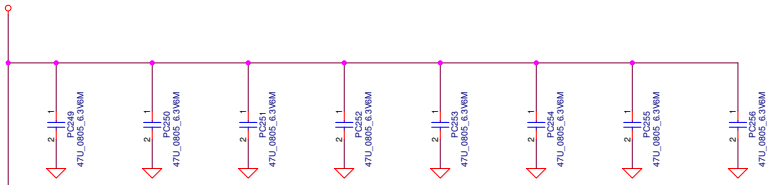
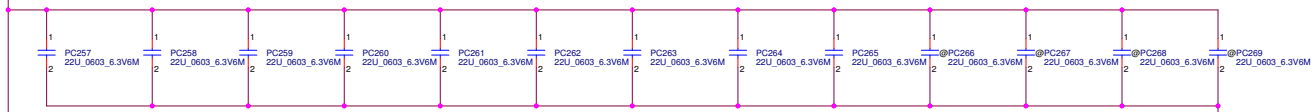
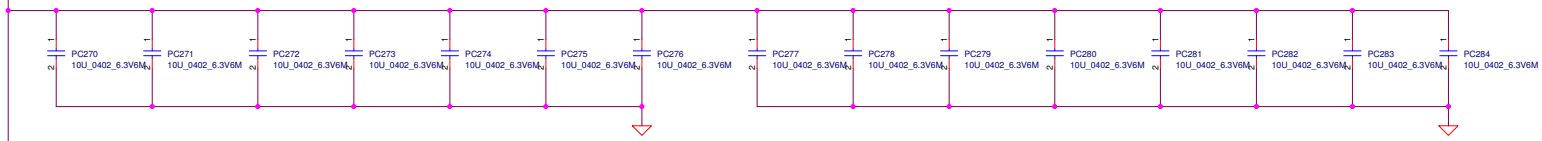
+VCC_CORE
220U_R9 * 3 pcs
47U_0805 * 8 pcs
22U_0603 * 9 pcs
10U_0402 * 7 pcs
1U_0201 * 26 pcs

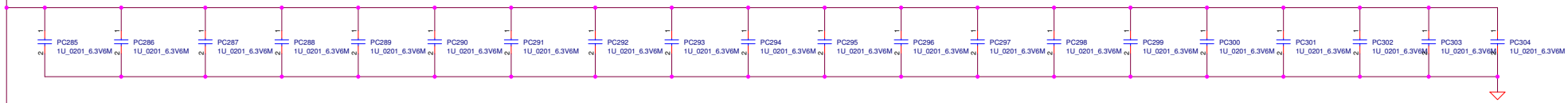
PPVAR_VCC

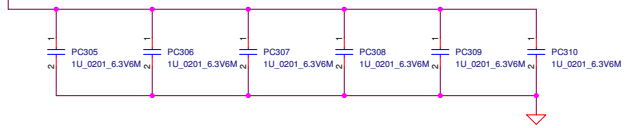


CAPS PLACE ON OPPOSITE SIDE OF SOC







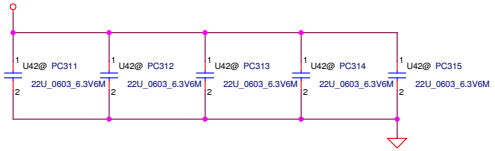


Jumper Footprint: SOLDER_PREFORMS_0805

PPVAR_VCC **PPVAR_GT_VCC**

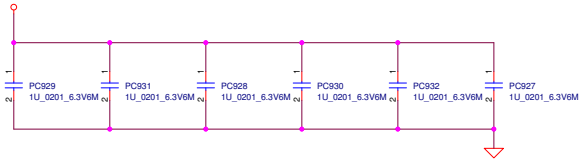
For KBL-R U42: PJCPU1
For KBL-U22: PJCPU2

PPVAR_VCC



Based on Intel PDG recommand

PPVAR_GT_VCC



Security Classification	Compal Secret Data		
Issued Date	2016/05/02	Deciphered Date	2018/12/31

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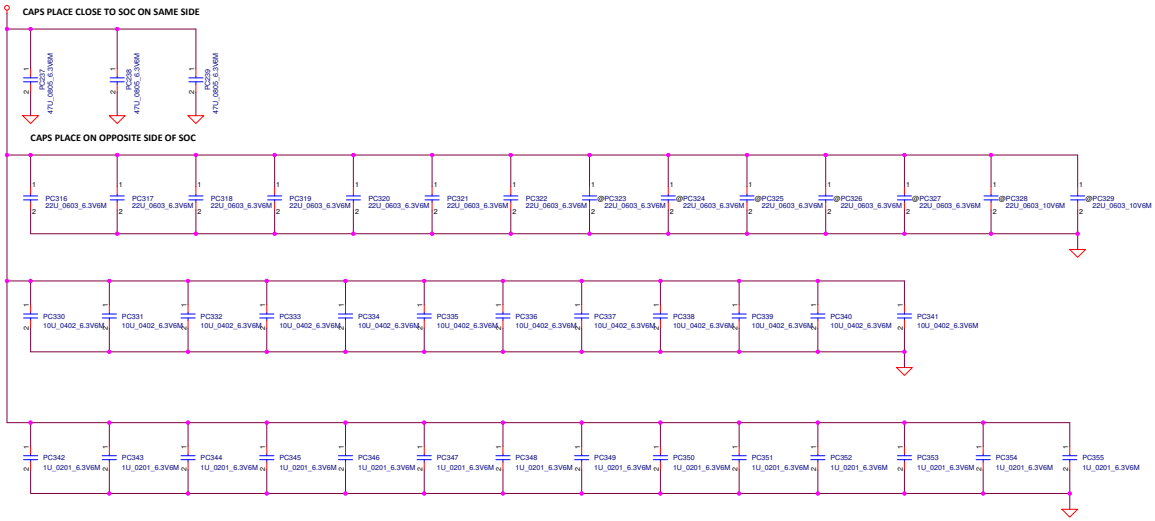
Compal Electronics, Inc.			
Title: CPU : CPU POWER (1/2)			
Size: Custom	Document Number		Rev: 0.1
Date: Thursday, July 19, 2018	Sheet 50 of 54		

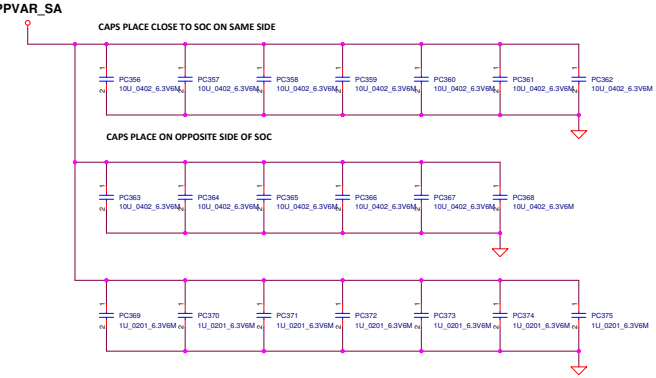
+VCC_GT
220U_R9 * 2 pcs
47U_0805 * 3 pcs
22U_0603 * 7 pcs
10U_0402 * 12 pcs
1U_0201 * 14 pcs

PPVAR_GT



+VCC_SA
10U_0402 * 13 pcs
1U_0201 * 7 pcs

PPVAR_SA



Security Classification	Compal Secret Data		
Issued Date	2016/05/02	Deciphered Date	2018/12/31

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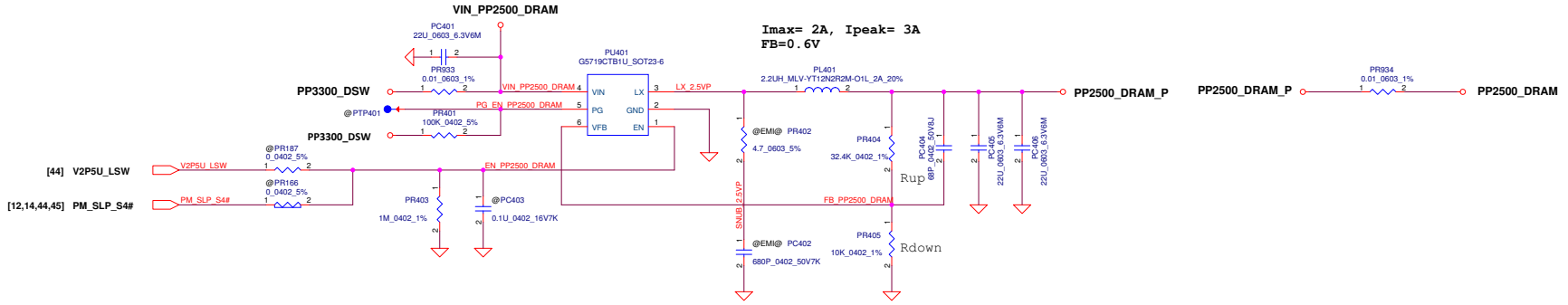
Compal Electronics, Inc.

Title: CPU : CPU POWER (2/2)

Size: Custom | Document Number | Rev 0.1

Date: Thursday, July 19, 2018 | Sheet 51 of 54

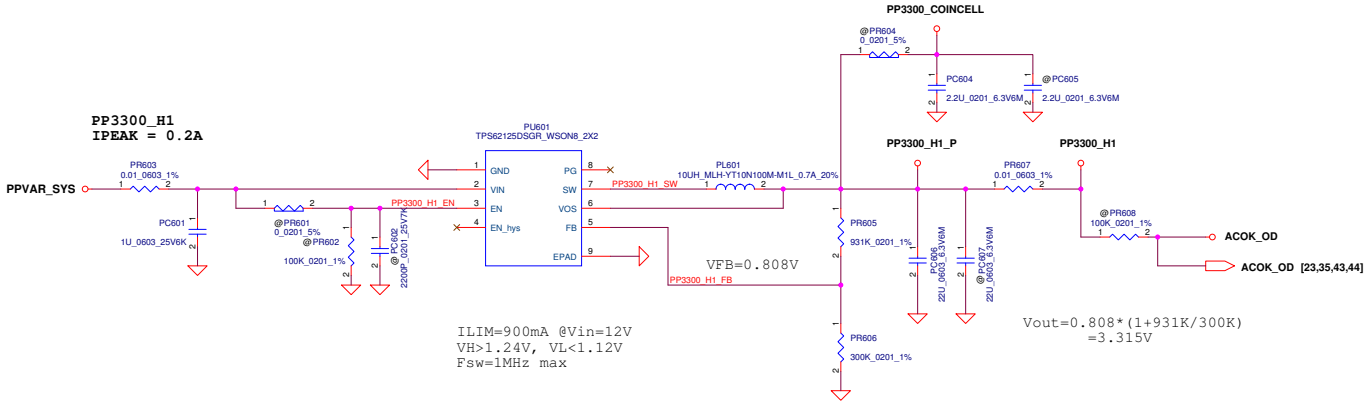
Change PP2500_DRAM solution from G9661 to G5719 for Intel Deep S3 mode



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Vout=2.544V



Security Classification	Compal Secret Data		
Issued Date	2016/05/02	Deciphered Date	2018/12/31

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Compal Electronics, Inc.			
Title: PWR 2.5VP			
Size: Custom	Document Number		Rev: 0.1
Date: Thursday, July 19, 2018	Sheet 52 of 54		

Version change list

Item	Reason for change	PG#	Modify List	Date	Phase
1	Follow reference board design	43	Charger VDD/VDDP Cap down size portion. (Reserve PC1,PC2 and change PC28/PC29 from 1uF to 2.2uF)	4/19	FVT
2	Follow reference board design	44	Install PR105 pull 100K to PP1000_VCCST.	4/19	FVT
3	Follow reference board design	52	Modify PP3300_H1 IC solution from G922 to TPS62125 by Google request.	4/23	FVT
4	Follow reference board design	42	Change PR477 from 0 ohm to 1K ohm prevent abnormal contact. Add PRB01/PRB02 100 ohm on BATT I2C for Battery connector. Add PQ62 Resistor PRB03 prevent abnormal contact.	5/4	FVT
5	Follow reference board design	45	PR137 change to 0.01 ohm from 0 ohm for HW power consumption test	6/4	SIT
6	Follow reference board design	52	Add PR603 & PR607 for HW power consumption test	6/4	SIT
7	Follow reference board design	52	PL401 change to 2.2uH	7/10	SVT
8	Compal rule	43 44 45 47 48 49 52	PR5, PR10, PR13, PR14, PR16, PR17, PR20, PR112, PR119, PR122, PR126, PR943, PR129, PR130, PR131, PR132, PR134, PR139, PR141, PR142, PR144, PR146, PR147, PR148, PR153, PR154, PR155, PR157, PR161, PR162, PR165, PR931, PR1236, PR34, PR41, PR42, PR53, PR54, PR65, PR75, PR82, PR172, PR173, PR176, PR177, PR178, PR84, PR85, PR89, PR90, PR94, PR95, PR101, PR103, PR166, PR601, PR604 change to short pad.	7/10	SVT
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

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Compal Electronics, Inc.			
Title	PWR-PIR		
Size: Custom	Document Number: LA-C423P		Rev: 1.0
Date: Thursday, July 19, 2018	Sheet 53 of 54		

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/11/23

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Compal Electronics, Inc.			
Title	Change List		
Size: Custom	Document Number		Rev: 0.1
Date: Thursday, July 19, 2018	Sheet 53 of 54		

Item	Page	Function/Signal/Parts	Change Descrption	Modified date
			Proto change list	
1	42	PJPB1	Change PJPB1 to 10pin connector.	2018/3/12
2	24	JTP1	Change JTP1 to 6pin connector.	2018/3/12
3	37	JKB1	Reverse JKB1 pin definition	2018/3/19
4	7	RAM ID	Update RAM ID and BOM structure	2018/3/19
5	24, 31	Power button LED	Add power button LED control signal PWRBTN_LED# from U89.A2 to R965.1 Net name EC_CHG_LED_W_R1 change to PWRBTN_LED_R#	2018/3/21
6	8	DDR select	RC230 un-stuff, RC231 stuff, and chane to 1k.	2018/3/21
7	40	PP3300_USB_PD	R385 un-stuff, R960 stuff	2018/3/22
8	40	Touch screen power	R5041 un-stuff, R5042 stuff	2018/3/22
9	12	VCCST_PWRGD	R95 stuff, PR105 un-stuff	2018/3/23
10	36	JTP1	Change JTP1 to 6pin pitch=0.5mm connector.	2018/3/23
11	14	VCCPLL_OC	Add CC118 for VCCPLL_OC by intel request	2018/3/23
12	22	R5087	Add PU 10k by google request	2018/3/26
13	33	0.1U 25V K X5R 0201	C24,C27 SE00001AA00 change to SE00001AAZ0	2018/3/26
14	14	0_0201_1%	RC27, RC30 change to 0_0201_5%	2018/3/26
15	15	C375	C375 change to 0.1U by RF request	2018/3/27
16	15	RC35	RC35 change to BLM18BG221SN1D_0603 by RF request	2018/3/27
17	9,12	ESD component	CC2, CC112, CC113, CC109, CC111, CC110, CC114, CC115 change to stuff by ESD request	2018/3/27
18	14	CC106	CC106 un-stuff by Intel request	2018/3/27
			EVT change list	
19	37	L1	PN change to SH000004MX00 to follow Nami design	2018/4/18
20	37	KB backlight	Add KBL@ for KB backlight BOM config	2018/4/18
21	15	CC77	Unstaff CC77 to meet intel sequence spec	2018/4/18
22	22	R5087/ WARM_RESET#	Add resistor 100K (R5087) PU to PP3300_A for WARM_RESET#	2018/4/18
23	20	RD94/ DDR_B_ALERT#	Change RD94 Compla PN(from SD000014400 to SD000007000)	2018/4/18
24	19, 20	RD18/RD65	Change RD18, RD65 Compal PN(from SD000015N80 to SD000012B80)	2018/4/18
25	12	C348/349	Change C348, C349 from 10P to 15P for crystal tuning	2018/4/18
26	23	R173	Unstaff R173 (EC don't control reset from H1)	2018/4/18
27	24	U103	Change U103.7 net form EC_WP# to PCH_WP for EEPROM	2018/4/18
28	25	RP1,RP2/ R5088~R5095	20k resistor pack (SD300003U00) change to 20k_0201 (SD000007G00)	2018/4/19
29	28	F1	1.1A fuse (SP040007U00) change to 1.5A fuse (SP040001G00)	2018/4/19
30	24	RP3,RP4/ R5096~R5103	4.7k resister pack (SD309470180) change to 4.7k_0201 (SD043470180)	2018/4/19
31	8	RPC1/ RC240~RC243	2.2k resistor pack (SD309220180) change to 2.2k_0201 (SD000012B80)	2018/4/19
32	13	RPC2/ RC235~RC238	10k resister pack (SD309100280) change to 10k_0201 (SD043100280)	2018/4/19
33	29, 30, 37	C381, C595, C4989	0.1u_0402 (SE095104K80) change to 0.1u_0201 (SE00000SV00)	2018/4/19
34	37	C596, C597	1u_0603 (SE000011W00) change to 1u_0402 (SE000010V00)	2018/4/19
35	19, 20	CD6, CD48, CD49, CD50, CD51, CD55, CD56, CD57, CD60, CD62	1u_0201 Compal PN SE00000YB00 change to SE00000UC00	2018/4/19
36	23	C369	1u_0402 (SE00000QL10) change to 1u_0201 (SE00000UC00)	2018/4/19
37	25, 28, 37	C72, C73, C237, C291, C4952	4.7u_0603 (SE00000MA00) change to 4.7u_0402 (SE00000ZY80)	2018/4/19
38	14, 15, 19, 20, 40	C579, CC4, CC5, CC9, CC14, CC16, CC19, CC27, CC29, CC30, CC37, CC38, CC39, CC40, CC41, CC42, CC51, CC54, CC55, CC56, CC60, CC61, CC62, CC63, CC64, CC65, CC66, CC67, CC69, CC70, CC73, CC74, CC78, CC79, CC106, CC116, CD2, CD3, CD4, CD5, CD9, CD10, CD11, CD12, CD13, CD14, CD15, CD16, CD18, CD19, CD20, CD23, CD24, CD28, CD29, CD30, CD31, CD32, CD33, CD34, CD35, CD38, CD39, CD42, CD43, CD45, CD46, CD53, CD54, CD58, CD59, CD63, CD64, CD65, CD70, CD71, CD74, CD75, CD76, CD77, CD78, CD79, CD80, CD81, CD84, CD85, CD88, CD89, CD91, CD92	1u_0402 (SE00000QK80) change to 1u_0201 (SE00000UC00)	2018/4/19
39	43	PC1, PC2, PC28, PC29	Reserve PC1,PC2 and change PC28/PC29 from 1uF to 2.2uF	2018/4/22
40	44	FR105	Install FR105 pull 100K to PP1000_VCCST	2018/4/22
41	7	EMMC	Add SANDISK_64G_1@ SA0000B4R00	2018/4/22
42	7	RAM	Add MICRON4G@, HYNIX_4G_1@ RAM	2018/4/22
43	52	PD601	Modify PP3300_H1 IC solution from G922 to TPS62125 by Google request	2018/4/23
44	11, 15, 29, 30, 40	C263, C352, C353, C354, C355, C356, C578, C581, C4987, C4990, CC105	0.01u_0201 Compal PN SE172103R80 cahnge to SE00000YH00	2018/4/23
45	34	LED1	Changed LED pull up to PP3300_DSW_EC	2018/4/25
46	12	C3/C4	Change C3, C4 from 10P to 7P for crystal tuning	2018/4/25
47	21	Q78/R5104/R5105/R5017	Add circuit for EEPROM WP solution	2018/4/25
48	24	U103	Rename U103.7 netname to SKU_WP_R	2018/4/25
49	21	R5107	Rename R5107.2 to SKU_WP_R	2018/4/25
50	12	RC70/ CC97/CC98	Change RC70/ CC97/CC98 package to 0201	2018/4/25
51	32	Q79/Q80/Q81/R5110	Adding circuit to isolate the SBU signals from type-C connector to TCPC in order to support CCD	2018/4/25
52	29	JNGFF1	Del JNGFF1 and around circuit	2018/4/25
53	34	D35	D35 change to FUSB3F64 (SCA00003W00) by ESD request	2018/4/26
54	34	D38	D38 change to AZC099-04S.R7G (SC300001G00) by ESD request	2018/4/26
55	24	R271, R5067	0.01_0402(SD00001UN00) change to 0_0402(SD028000080)	2018/4/27
56	34	R4998/R22	R4998 change to 1.2k ohm, R22 change to 200 ohm for LED brightness tuning.	2018/4/29
57	24, 35	R5111	Add R5111 between EC_RST_ODL and EC_WCC1_RST	2018/4/30
58	35	U91	U91 Compal PN change to SA0000BLL20 for FW update	2018/4/30
59	37	U88	Follow Nami U88 pin4&8 change to PP5000_A	2018/5/2
60	24	R4941/R4942	R4941, R4942 change to 2.2k	2018/5/2
61	42	PR477 PRB01/PRB02 PQ62/PRB03	Change PR477 from 0 ohm to 1K ohm prevent abnormal contact. Add PRB01/PRB02 100 ohm on BATT I2C for Battery connector. Add PQ62 Resistor PRB03 prevent abnormal contact.	2018/5/4
62	34	R22/R4998	Updated R22 to 1.2K-ohm (white color), R4998 to 200-ohm (amber) for tune brightness	2018/5/6
63	38	R4976/ R4977	Change R4976, R4977 to 3.3K and unstuff.	2018/5/6
64	32	C4973 ~ C4980 C4983 ~ C4986	Removed C4973 ~ C4980 for DP; C4983 ~ C4986 for USB3 (follow vendor reference schematic)	2018/5/6
65	37	C379	Change C379 power rail change to PP5000_A	2018/5/6
66	40	U53/R386/C319	Unstuff U53/R386/C319 for reserve path PP3300_USB_PD	2018/5/6
67	32	R5072/R5073 DP1_AUXP_SBU1; DP1_AUXN_SBU2	Removed R5072 and R5073 from DP1_AUXP_SBU1, DP1_AUXN_SBU2	2018/5/6
68	35	U91	Updated U91 reset IC Pin Configuration	2018/5/6
69	24	R5112	Add reserve R5112 100K PU to PP3300_H1 for TABLET_MODE	2018/5/6
70	34	LED1	Changed LED1 power rail to PP3300_DSW	2018/5/6
71	37	R829	Changed R829 from 2.2K to 8.06K for ILED max setting	2018/5/6
72	24	R5113~R5116	Add R5113~R5116 reseved circuit connect to EC_I2C_3	2018/5/6
73	10, 12, 15	C374/C375/C376	C374,C375,C376 change to 3.3p by RF request	2018/5/6
74	37	U88	U88 pin4 VIO change to PP3300_DSW_EC	2018/5/6
75	37	Keyboard	Reverse JKB1 pin define.	2018/5/9
76	12, 25	C4914, C4915, C348, C349, CC97, CC98	15p_0201_50V change to 15p_0201_25V for material shortage	2018/5/11
77	15	RC35	0ohm chane to bead BLM18BG221SN1D by RF request	2018/5/11
78	15	C374, C375	3.3p_0201_25V change to 2p_0201_25V for material shortage	2018/5/11
79	10	C376	3.3p_0402_50V change to 2p_0402_50V for material shortage	2018/5/11
			DVT change list	
80	24	U103	Rename EC_I2C_0_SCL_R>>HW_ID_I2C_SCL EC_I2C_0_SDA_R>>HW_ID_I2C_SDA to follow Nami's name	2018/6/1
81	13, 31	EMR_GARAGE_DET EMR_GARAGE_DET_GPP_E1 EMR_GARAGE_DET_GPP_E8	Rename EMR_GARAGE_DET# to EMR_GARAGE_DET for GME; EMR_GARAGE_DET#_GPP_E1 to EMR_GARAGE_DET_GPP_E1; EMR_GARAGE_DET#_GPP_E8 to EMR_GARAGE_DET_GPP_E8 (Switch is normal close)	2018/6/1
82	23	H1 SECURE	Add note for H1 strap	2018/6/1
83	37	R829	Follow test result change R829 to 8.2K for KB_BL ILED MAX	2018/6/1
84	32	PP3300_USB_PD PP3300_USB_PD_ANX_AVDD PP3300_USB_PD_ANX_DVDD ROLE_SELECT SOC_DP1_AUXP/N_C TEST_EN FF0/FF1	Changed power design: PP3300_USB_PD > PP3300_USB_PD_ANX_AVDD > PP3300_USB_PD_ANX_DVDD by vendor suggestion to make sure the AVDD33 power is no later than DVDD_IO. Changed ROLE_SELECT PU power rail to PP3300_USB_PD_ANX_AVDD by vendor suggestion. Change DP AUX PU/PD throught capacitor in MUX side. Remove TEST_EN, FF0 and FF1 testpoint by vendor suggestion to make them as NC.	2018/6/1
85	36	UT1 R5125/R5126	Remove UT1 I2C bus PU resistor RT1 and RT2. (Already PU on EC side) Change UT1 VCC to PP3300_DSW and reserve PP3300_S path.	2018/6/1
86	23	USB_C1_SBU1/USB_C1_SBU2 R5127/R5128 R797/R798	Add note for CCD mode Add R5127 and R5128 1M PD on H1 CC1/CC2 to prevent detecting Add if there isn't SuzyQ cable connected Change R797 and R798 to 0 ohm	2018/6/1
87	23	R841/R842	Stuff R841/R842 to enable SuzyQ	2018/6/1
88	13, 29, 30	R5136/R5137/R5138/R5139/C5004/C5005	Connect GPP_E4 for BT_OFF# to JWLN1.54, (JNGFF.54). Connect GPP_E2 for WLAN_OFF# to JWLAN1.56 (JNGFF1.56). Add 0 ohm for debugging and add cap for filtering.	2018/6/3
89	24, 32, 40	R5051/R5052/R877/R510/R5101/R5056/R5059/R5135/C5008	Stuff R5051/R5052 and pull up to PP3300_USB_PD_ANX_DVDD. Full up R5056/R5059/R877 to PP3300_USB_PD_ANX_DVDD. Unstuff R5100/R5101. Reserve R5135/C5008	2018/6/3
90	37	D14	Change D14 PCB FootPring to "ESD101-B1-02ELS_TSSLP-2-4-2"	2018/6/3
91	24, 32	R5140 TP927	Add 0 ohm resistor R5140 net to U115.46 & "USB_C1_PD_RST_ODL" Add test point TP927 net to U115.45	2018/6/3
92	31, 33	R5141/R5143/U27/U33	Change U33.8 net to "PP3300_BC12_C1_VDDIO" ; add R5141 net to "PP3300_BC12_C1_VDDIO" change U27.8 net to "PP3300_BC12_C0_VDDIO" ; add R5143 net to "PP3300_BC12_C0_VDDIO"	2018/6/3
93	24	R5145/R5146/R4941/R4942	Add R5145 net to "EC_I2C_0_SCL"; R5146 net to "EC_I2C_0_SDA" Unstuff R4941/R4942	2018/6/3
94	24	R5147/R5148	Add reserve resistor R5148 net to "PP3300_DSW_EC" & U103.8 ; Add resistor R5147 net to "PP3300_USB_PD" & U103.8	2018/6/3
95	24, 32	R5151/R5152/R5153	Add reserve resistor R5151 net to "USB_C0_PD_INT_ODL" & "PP3300_DSW_EC"; Add reserve resistor R5152 net to "USB_C0_PD_RST_ODL" & "PP3300_DSW_EC"; Add reserve resistor R5153 net to "USB_C1_PD_RST_ODL" & GND	2018/6/3
96	33	DP1_AUXP_SBU1/DP1_AUXP_SBU2 USB_C1_SBU1/USB_C1_SBU1	change "DP1_AUXP_SBU1" to "USB_C1_SBU1" from JTYPEC1.A8 to D40.4/D40.7 change "DP1_AUXP_SBU2" to "USB_C1_SBU2" from JTYPEC1.B8 to D40.4/D40.7	2018/6/3
97	23	R841/R842	Change R841 and R842 BOM Structure to MP@	2018/6/3
98	28	R5085/R5086/C323/C324/C372/C371	Unstuff R5085/R5086/C323/C324/C372/C371	2018/6/3
99	28	F1	Change back 1.1A fuse (SP040007U00) to follow Nami	2018/6/3
100	33, 34	D20/ D38	D20, D38 change to AZC099-04S (SC300005Y00) by ESD request	2018/6/3
101	45	PR137	PR137 change to 0.01 ohm from 0 ohm for HW power consumption test.	2018/6/4
102	52	PR503/PR507	Add PR503 & PR507 for HW power consumption test.	2018/6/4
103	47, 52	PU2/PU601/PL601	Re-link PU2 & PU601 & PL501 for Compal Symbols released.	2018/6/4
104	32	R5117 ~ R5124, R5129 ~ R5132	Reserve R5129 ~ R5132 for USB3 by intel recommend; Add net USB3_CTX_MR_P/N2_R, USB3_CRX_MTX_P/N2_R for U115 USB3 port Reserve R5117 ~ R5124 for DP by intel recommend; Add net SOC_DP1_P/N[0:3]_R for U115 DP port	2018/6/5
105	31	JI02	Add R5149 and reserve R5150 for sub board PS8751 power	2018/6/5
106	12	R95	Unstuff R95 due to PR105 already pull-high.	2018/6/6
107	24	R5112	Stuff R5112	2018/6/7
108	23	R841/R842	Change R841 and R842 BOM Structure form MP@ to CCD@ for CCD mode enable	2018/6/7
109	35	U91	Update reset IC PN from FW005 to FW006(SA0000BLL30) and Pin Configuration table	2018/6/7
110	32	U115	Update U115 PN from ANX7447 to ANX3447(SA0000C9000)	2018/6/7
111	30	R5136/ R5137	Un-stuff R5136, R5137	2018/6/14
112	21	R5104	100k ohm change to 3.3k ohm	2018/6/14
113	30, 40	C260/C589	C260 change to 47U, C589 change to 22U for WLAN power rising time tuning	2018/6/19
114	11	L20/R4952	L20,R4952 unstuff for rear camera not support	2018/6/19
115	21	R5104/U103	Change R5104 from 3.3K to 1K for SKU_WP_R voltage level (depend on U103.7 internal PD)	2018/6/19
116	23, 32, 33	USB_C1_CC1/2 USB_C0_CC1/2 to USB_C1_CC1_H1/2	Change netname USB_C1_CC1_H1/2 to USB_C1_CC1/2; USB_C0_CC1/2 to USB_C1_CC1_H1/2	2018/6/19
			FVT change list	
117	24, 36	R5154/R4918 USB2_ID_EC TP950	Change net USB2_ID_EC from GPI057 to GPI042 and add R5154 for OTG function. Unstuff R4918; Add Testpoint TP950 reserve for GPI057	2018/7/11
118	23	R797/R798/R5127/R5128	Change R797 and R798 from 0 ohm to 1K ohm; Unstuff R5127 and R5128.	2018/7/11
119	32	R5155/R5156 R5110/Q79/Q80/Q81/D42	Add reserve 0 ohm R5155 and R5156 for non-CCD mode Add note and BOM Structure for CCD mode option	2018/7/11
120	24	R5111	Unstuff R5111 for reset IC PW006	2018/7/11
121	37	R829	8.2K_0201_1% (SD00000B880) change to 8.2k_0201_5% (SD043E20180) by purchaser request.	2018/7/11
122	52	FL401	FL401 change to 2.2uH	2018/7/12
123	42~52	PR5, PR10, PR13, PR14, PR16, PR17, PR20, PR112, PR119, PR122, PR126, PR943, PR129, PR130, PR131, PR132, PR134, PR139, PR141, PR142, PR144, PR146, PR147, PR148, PR153, PR154, PR155, PR157, PR161, PR162, PR165, PR931, PR1236, PR84, PR41, PR42, PR53, PR54, PR85, PR75, PR82, PR172, PR173, PR176, PR177, PR178, PR84, PR85, PR89, PR90, PR94, PR95, PR101, PR103, PR166, PR601, PR604	0ohm change to short pad	2018/7/12
124		0201 R4917, R4916, RC6, R961, R962, R56, R4928, R929, R934, R4910, R105, R950, RC228, RC229, RC21, RC22, RC30, RC28, RC27, RC24, RC234, RC56, RC46, R5105, R136, R137, R138, R124, R125, R835, R834, R213, R214, R160, R190, R196, R176, R182, R188, R180, R202, R177, R196, R197, R194, R195, R171, R206, R837, R840, R966, R904, R968, R301, R5113, R5114, R965, R5096, R33, R5026, R5035, RC222, R4924, R332, R5143, R5117, R5118, R5119, R5120, R5121, R5122, R5123, R5124, R5129, R5130, R5131, R5132, R5140, R4926, R5048, R5141, R345, R4948, R970, R4919, R5126, R5042, R936, R953, R854, R855, R849, R848, R860, R853, R856, R862, R866, R47, R48, R46, R4989, R139, R5037 0402 RC110, RC25, RC33, RC51, R271, R5004, R5002, R5009, R5067, RC57,	0ohm change to short pad	2018/7/12
125	7	PCB Compal PN	PCB Compal part number change to K3 part number (DAA000HP010)	2018/7/13
126	7	U14	EMMC Compal part number change to K3 part number SA0000C0810 (Sandisk 32G), SA0000B4R10 (Sandisk 64G), SA0000BPX10 (Hynix 128G), SA0000BPN10 (Sandisk 128).	2018/7/13
127	7	UD1-UD8	DDR Compal part number change to K3 part number SA0000B6F10 (Samsung 8G), SA0000BMN10 (Hynix 8G), SA0000ARD30 Micorn 8G)	2018/7/13
128	21, 33	D59, D60	Reserved D59,D60 (SMF4L20A) TVS by Nami team request.	2018/7/17
129	21, 22, 30	D2, D4, D8, D9, D24	Change 2nd source RB520S30 (SC00000AQ00) to main source RB520SM (SC00000C000) by sourcer request	2018/7/18

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